IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS,
LUFKIN DIVISION

SAMSUNG ELECTRONICS CO., LTD., §
§
Plaintiff, §
§
V. §
§
SANDISK CORPORATION, §
§
Defendant. §

CIVIL ACTION NO. 9:02cv58

Judge Hannah

COMPLAINT

Samsung Electronics Co., Ltd., complains of SanDisk Corporation for violations of the United States patent laws. In support of its complaint, Samsung alleges as follows:

PARTIES

1. Samsung Electronics Co., Ltd., ("Samsung") is a company organized under the laws of South Korea with its principal place of business located at 416 Maetan-3 Dong, Paldal-Gu, Suwon City, Kyungki-Do, Korea.

2. On information and belief, SanDisk Corporation ("SanDisk") is a company organized under the laws of Delaware with its principal place of business in Sunnyvale, California. SanDisk may be served with process by serving Mr. Sanjay Mehrotra, Chief Operating Officer & Executive Vice President, SanDisk Corporation, 140 Caspian Court, Sunnyvale, California 94089.

JURISDICTION

3. This is an action arising under the United States patent laws, 35 U.S.C. § 101 *et seq*. This Court has subject matter jurisdiction under 35 U.S.C. §§ 271, 281, and 28 U.S.C. § § 1331 and 1338 (a).

VENUE

4. Venue over Samsung's claims is proper in this district pursuant to 28 U.S.C. §§ 1391(b)-(c), and 1400(b) because SanDisk resides in this judicial district and part of Samsung's causes of action arose in this judicial district.

BACKGROUND FACTS COMMON TO ALL CLAIMS

5. Samsung is the world's leading manufacturer of semiconductor memory products. Samsung currently manufactures, distributes and sells dozens of memory products throughout the world, including the United States. One of these memory products is the NAND Flash card, which is commonly referred to in the industry as a flash memory product.

6. Flash memory products are typically removable memory cards that are often found in digital cameras, digital music players, digital camcorders, handheld PCs, e-Books, and newer cellular phone technology, as well as other emerging products.

7. SanDisk manufactures and supplies flash memory products in consumer, OEM, and industrial markets. More specifically, SanDisk supplies, at least, the CompactFlash™ commercial flash memory product line that infringes upon one or more United States patents that are owned by Samsung. SanDisk also distributes other products that infringe at least some of Samsung's patents.

8. SanDisk directly sells its memory products around the world and through intermediaries, including wholesalers, distributors, value-added resellers, and retailers located throughout the United States and specifically in this judicial district. Retailers of SanDisk products include Circuit City, K-Mart, Office Depot, Target, Sears, Office Max, Staples, Eckerd drug stores and Walgreens drug stores, among others.

9. SanDisk also sells its flash memory products to and through original equipment manufacturers ("OEMs"), including Cannon, Hewlett-Packard, Fujitsu, Motorola, Kodak, Panasonic, and Polaroid, among others. SanDisk also sells flash memory products to private label partners that re-brand the SanDisk products under a different trade name, which are then sold directly to consumers or installed into consumer products.

10. As part of its sales of memory products in the United States, SanDisk markets, promotes, sells and offers for sale a full range of its flash memory products in Texas. SanDisk markets its flash memory products in Texas by using a direct sales organization and numerous distributors and manufacturers' representatives. In fact, SanDisk even has a direct sales office in Texas to support its OEM customers and its distribution and manufacturer representatives.

11. On information and belief, SanDisk flash memory products, including the CompactFlash™ product line, have been sold and are currently being sold on Amazon.com's internet website, which is available to consumers residing in the Lufkin Division. On information and belief and according to information provided by Amazon.com, based on purchases made via the Amazon.com internet website, the SanDisk 128MB CompactFlash™ card ranks among the top selling electronic products purchased by consumers in Texas. SanDisk and Amazon.com do not restrict or otherwise

prevent consumers residing in the Lufkin Division from purchasing SanDisk flash memory products on the Amazon.com internet website.

12. On information and belief, SanDisk directly markets, promotes, sells, offers for sale, or leases its flash memory products, including the CompactFlash™ product line, in numerous locations throughout the Lufkin Division of the Eastern District of Texas ("Lufkin Division"). On information and belief, SanDisk also markets, promotes, sells, offers for sale, or leases its flash memory products, including the CompactFlash™ product line, in numerous locations throughout the Lufkin Division by way of intermediaries, such as wholesalers, distributors, value-added resellers and retailers.

13. SanDisk has sold and is currently selling a full range of its flash memory products in the Lufkin Division. The SanDisk flash memory products being sold in the Lufkin Division include the CompactFlash™ product line. SanDisk is selling these products either directly or indirectly through wholesalers, distributors, or value-added resellers, to various retail outlets located in Angelina and Nacogdoches Counties. These flash memory products are in turn sold to consumers and end-users of the flash memory products who reside in the Lufkin Division.

14. On information and belief, SanDisk flash memory products, including the CompactFlash™ product line, have been sold and are currently being sold in Lufkin, Angelina County, Texas at the following retail outlets: Sears, which is located at the Lufkin Mall, 4600 S. Medford Dr., Lufkin, Texas 75901; Walgreens drugstore, which is located at 102 N. Timberland Dr., Lufkin, Texas 75901; two Eckerd drugstores, which are located at 1204 E. Lufkin Avenue, and at 923 Frank Street, Lufkin, Texas 75901; Target, which is located at 4200 S. Medford Drive, Lufkin, Texas 75901; Circuit City,

which is located at 4600 S. Medford Drive, Lufkin, Texas 75901; Office Depot, which is located at 4210 S. Medford Drive, Lufkin, Texas 75901; and OfficeMax, which is located at 2429 South John Reddit Drive, Lufkin, Texas 75901. Dozens, if not hundreds, of SanDisk products are offered for sale to consumers at these locations within the Lufkin Division. On information and belief, each of these retail outlets receive flash memory products either directly from SanDisk or indirectly through intermediaries, such as wholesalers, distributors or value-added resellers. On information and belief, under certain conditions, these retail outlets have the right to return any unsold SanDisk flash memory inventory directly to SanDisk, including any unsold products in the CompactFlash™ product line.

15. On information and belief, SanDisk products, including the CompactFlash™ product line, have been sold and are currently being sold in Nacogdoches, Nacogdoches County, Texas at the following retail outlets: Staples, which is located at 4608 North Street, Nacogdoches, Texas 75961; and Eckerd drugstore located at 1424 North Street, Nacogdoches, Texas 75961. Dozens of SanDisk products are offered for sale to consumers at these locations within the Lufkin Division. On information and belief, each of these retail outlets receive flash memory products either directly from SanDisk or indirectly through intermediaries, such as wholesalers, distributors or value-added resellers. On information and belief, under certain conditions these retail outlets have the right to return any unsold SanDisk flash memory inventory directly to SanDisk, including any unsold products in the CompactFlash™ product line.

16. On information and belief, SanDisk products, including products within the CompactFlash™ product line, have been incorporated into the following OEM products

that have been and are currently being sold in the Lufkin Division: Kodak digital cameras; Polaroid digital cameras; Nikon digital cameras; and Hewlett-Packard digital cameras.

17. On information and belief, SanDisk products, including the CompactFlash™ product line, are being promoted, advertised and offered for sale in the Lufkin Division. More specifically, SanDisk products have been promoted, advertised, and offered for sale in Walgreens circular advertisements that were included in Lufkin's newspaper, the Lufkin Daily News, on February 17, 2001. SanDisk also promotes, advertises and offers for sale its flash memory products on its internet website, which is described more fully in the following paragraphs.

18. On information and belief, SanDisk has knowingly and intentionally formed a channel of distribution for its flash memory products, including the CompactFlash™ product line, into the Lufkin Division. SanDisk knows or should have known that the Lufkin Division was a termination point of its distribution channel for flash memory products, including the CompactFlash™ product line.

19. On information and belief, SanDisk has offered cash rebates on sales of flash memory products sold to consumers in the United States. Cash rebates have been offered for SanDisk's flash memory products, including the CompactFlash™ product line, that were and are sold to consumers in the Lufkin Division. On information and belief, during SanDisk promotional events, consumers can ordinarily obtain rebate information and rebate certificates for SanDisk's products directly from the retail outlets located in the Lufkin Division that sell SanDisk flash memory products, including the

CompactFlash™ product line. This information can also be obtained on SanDisk's internet website, which is described more fully in the following paragraphs.

20. On information and belief, SanDisk has offered and continues to offer warranties on its flash memory products sold to consumers in the United States. Warranties have been offered and continue to be offered on SanDisk's flash memory products, including the CompactFlash™ product line, to consumers residing in the Lufkin Division. On information and belief, consumers can obtain warranty information and warranty registration materials for SanDisk's products from the retail outlets located in the Lufkin Division that sell SanDisk flash memory products, including the CompactFlash™ product line. On information and belief, SanDisk warranty information and warranty registration materials for SanDisk's flash memory products are included within the package of each retail SanDisk product sold. This information can also be obtained on SanDisk's internet website, which is described more fully in the following paragraphs.

21. On information and belief, SanDisk offers a five-year warranty on all of its flash memory products, including products in the CompactFlash™ product line. The SanDisk warranty provides that SanDisk "will repair or replace this Flash Memory Card free of charge if it ever fails within 5 years from the date of purchase. . . SanDisk will inspect the product and at its option, repair or replace the product. SanDisk will ship out a product with equal or greater capacity."

22. The SanDisk warranty registration material on its flash memory products, including the CompactFlash™ product line, which is enclosed within the package of each retail product, require the consumer to complete a mail-in card enclosed with the product and mail the registration materials to SanDisk's Warranty Registration division. This

warranty registration material refers consumers to SanDisk's internet website, which is described more fully in the following paragraphs.

23. On information and belief, SanDisk engages in substantial e-commerce by way of the internet and does business in the Lufkin Division through its interactive website, which is located at http://www.sandisk.com/main.htm.

24. SanDisk's website is highly interactive in its promotion, advertising and marketing of SanDisk's flash memory products. The SanDisk website allows consumers to shop for, order and purchase a full range of SanDisk's flash memory products. Consumers in Texas, including consumers residing in the Lufkin Division, have purchased SanDisk's flash memory products, including products from the CompactFlash™ product line, through SanDisk's internet website. SanDisk does not restrict or otherwise prevent consumers residing in the Lufkin Division from purchasing SanDisk's flash memory products on its website.

25. SanDisk has shipped flash memory products, including products from the CompactFlash™ product line, purchased through SanDisk's website to consumers residing in the Lufkin Division.

26. SanDisk's website provides consumers with warranty information related to its flash memory products, including its CompactFlash™ product line. *See* http://www.sandisk.com/tech/rw_cf.asp. SanDisk does not restrict or otherwise prevent consumers residing in the Lufkin Division from initiating warranty claims or obtaining warranty information about SanDisk's flash memory products from its website.

27. SanDisk allows consumers to register warranty information for its flash memory products, including products from the CompactFlash™ product line, through its website.

See http://www.sandisk.com/tech/prod-reg.asp. To register a flash memory product for warranty purposes, the consumer must complete several fields of inquiry and provide requested information to SanDisk, including the consumer's residence and where the SanDisk product was purchased. *See Id.* SanDisk does not restrict or otherwise prevent consumers residing in the Lufkin Division from registering SanDisk's flash memory products on its website.

28. SanDisk's website provides consumers residing in the Lufkin Division with cash rebates and cash rebate information on its flash memory products. *See* http://www.sandisk.com/tech/rebates.asp. As can be seen from the SanDisk website, rebates are offered on various SanDisk products, including CompactFlash™ cards, and from various retail merchants. *See and click on the Circuit City hyperlink at* http://www.sandisk.com/tech/rebates.asp. SanDisk's website also instructs consumers on the proper procedure for obtaining a delayed rebate payment on any applicable SanDisk product. *See and click on hyperlink* "Why haven't I received by rebate yet?" at http://www.sandisk.com/tech/faq_search.asp. SanDisk does not restrict or otherwise prevent consumers residing in the Lufkin Division from obtaining rebates and rebate information on SanDisk's flash memory products from its website.

29. SanDisk invites consumers to interact with its technical support staff via e-mail or telephone with respect to customer service issues or technical support that consumers need for the proper operation and use of SanDisk's flash memory products, including the CompactFlash™ product line. *See* http://www.sandisk.com/tech/contact.asp. SanDisk does not restrict or otherwise prevent consumers residing in the Lufkin Division from

obtaining customer service information or technical support for SanDisk's flash memory products from its website.

30. SanDisk invites consumers to interact with its website by allowing consumers to "design products which use SanDisk cards, flash memory chips [including CompactFlash™ products] and other SanDisk technology." *See* http://www.sandisk.com/tech/oem_design/s_oem.asp. SanDisk does not restrict or otherwise prevent consumers residing in the Lufkin Division from interacting with the SanDisk website to design products that incorporate SanDisk's flash memory products.

31. SanDisk invites consumers to interact with its website by allowing consumers to download software upgrades for various consumer devices so that SanDisk's flash memory products, including products from the CompactFlash™ product line, are compatible with the consumer devices with which they are installed. *See* http://www.sandisk.com/tech/s_downloads.asp. On information and belief, certain consumer products will not function unless the consumer downloads the appropriate software (*e.g.*, drivers) from SanDisk's website. SanDisk does not restrict or otherwise prevent consumers residing in the Lufkin Division from interacting with the SanDisk website to download software so that SanDisk's flash memory products can be installed in consumer devices.

32. SanDisk invites consumers to interact with SanDisk by allowing consumers the option to enroll in SanDisk's quarterly product e-mail list that is distributed to consumers by SanDisk. *See* http://www.sandisk.com/tech/prod-reg.asp. SanDisk does not restrict or otherwise prevent consumers residing in the Lufkin Division from receiving SanDisk's quarterly product e-mail list.

33. As the preceding paragraphs show, SanDisk clearly does business in the Lufkin Division by virtue of its established channels of distribution and interactive website.

COUNT ONE
Infringement of United States Patent No. 5,473,563

34. Samsung incorporates by reference paragraphs 1 through 33 as though fully set forth herein.

35. Samsung is the sole owner of the entire right, title, and interest in United States Patent No. 5,473,563 ("the '563 patent"), which was duly and legally issued to Samsung on December 5, 1995, and entitled "Nonvolatile Semiconductor Memory." A copy of the '563 patent is attached hereto as Exhibit A.

36. Samsung has never licensed or permitted SanDisk to practice any of the claims granted in the '563 patent.

37. On information and belief, SanDisk has infringed the '563 patent, literally or by equivalents, by making, using, selling, offering for sale, leasing, or importing nonvolatile semiconductor memory products into the United States, including the Lufkin Division, that read on one or more of the inventions covered by the claims of the '563 patent. On information and belief, SanDisk continues to engage in such acts of infringement.

38. On information and belief, SanDisk, with full knowledge of Samsung's ownership interests in the '563 patent, has intentionally induced and is currently inducing others to infringe the '563 patent, or has contributed to the infringement of the '563 patent by actively and knowingly aiding and abetting others to make, use, sell, offer for sale, lease, or import nonvolatile semiconductor memory products into the United States, including

the Lufkin Division, that infringe one or more of the inventions covered by the claims of the '563 patent, either literally or by equivalents.

39. SanDisk's infringement of the '563 patent has been willful, and any further infringement of the '563 patent by SanDisk would be with full knowledge of Samsung's legal interest in the '563 patent and would be deliberate and willful.

COUNT TWO
Infringement of United States Patent No. 5,514,889

40. Samsung incorporates by reference paragraphs 1 through 39 as though fully set forth herein.

41. Samsung is the sole owner of the entire right, title, and interest in United States Patent No. 5,514,889 ("the '889 patent"), which was duly and legally issued to Samsung on May 7, 1996, and entitled "Non-Volatile Semiconductor Memory Device and Method for Manufacturing the Same." A copy of the '889 patent is attached hereto as Exhibit B.

42. Samsung has never licensed or permitted SanDisk to practice any of the claims granted in the '889 patent.

43. On information and belief, SanDisk has infringed the '889 patent, literally or by equivalents, by making, using, selling, offering for sale, leasing, or importing nonvolatile semiconductor memory products into the United States, including the Lufkin Division, that read on one or more of the inventions covered by the claims of the '889 patent. On information and belief, SanDisk continues to engage in such acts of infringement.

44. On information and belief, SanDisk, with full knowledge of Samsung's ownership interests in the '889 patent, has intentionally induced and is currently inducing others to infringe the '889 patent, or has contributed to the infringement of the '889 patent by

actively and knowingly aiding and abetting others to make, use, sell, offer for sale, lease or import nonvolatile semiconductor memory products into the United States, including the Lufkin Division, that infringe one or more of the inventions covered by the claims of the '889 patent, either literally or by equivalents.

45. SanDisk's infringement of the '889 patent has been willful, and any further infringement of the '889 patent by SanDisk would be with full knowledge of Samsung's legal interest in the '889 patent and would be deliberate and willful.

COUNT THREE
Infringement of United States Patent No. 5,546,341

46. Samsung incorporates by reference paragraphs 1 through 45 as though fully set forth herein.

47. Samsung is the sole owner of the entire right, title, and interest in United States Patent No. 5,546,341 ("the '341 patent"), which was duly and legally issued to Samsung on August 13, 1996, and entitled "Nonvolatile Semiconductor Memory." A copy of the '341 patent is attached hereto as Exhibit C.

48. Samsung has never licensed or permitted SanDisk to practice any of the claims granted in the '341 patent.

49. On information and belief, SanDisk has infringed the '341 patent, literally or by equivalents, by making, using, selling, offering for sale, leasing, or importing nonvolatile semiconductor memory products into the United States, including the Lufkin Division, that read on one or more of the inventions covered by the claims of the '341 patent. On information and belief, SanDisk continues to engage in such acts of infringement.

50. On information and belief, SanDisk, with full knowledge of Samsung's ownership interests in the '341 patent, has intentionally induced and is currently inducing others to infringe the '341 patent, or has contributed to the infringement of the '341 patent by actively and knowingly aiding and abetting others to make, use, sell, offer for sale, lease, or import nonvolatile semiconductor memory products into the United States, including the Lufkin Division, that infringe one or more of the inventions covered by the claims of the '341 patent, either literally or by equivalents.

51. SanDisk's infringement of the '341 patent has been willful, and any further infringement of the '341 patent by SanDisk would be with full knowledge of Samsung's legal interest in the '341 patent and would be deliberate and willful.

COUNT FOUR
Infringement of United States Patent No. 5,642,309

52. Samsung incorporates by reference paragraphs 1 through 51 as though fully set forth herein.

53. Samsung is the sole owner of the entire right, title, and interest in United States Patent No. 5,642,309 ("the '309 patent"), which was duly and legally issued to Samsung on June 24, 1997, and entitled "Auto-Program Circuit in a Nonvolatile Semiconductor Memory Device." A copy of the '309 patent is attached hereto as Exhibit D.

54. Samsung has never licensed or permitted SanDisk to practice any of the claims granted in the '309 patent.

55. On information and belief, SanDisk has infringed the '309 patent, literally or by equivalents, by making, using, selling, offering for sale, leasing, or importing nonvolatile semiconductor memory products into the United States, including the Lufkin Division,

that read on one or more of the inventions covered by the claims of the '309 patent. On information and belief, SanDisk continues to engage in such acts of infringement.

56. On information and belief, SanDisk, with full knowledge of Samsung's ownership interests in the '309 patent, has intentionally induced and is currently inducing others to infringe the '309 patent, or has contributed to the infringement of the '309 patent by actively and knowingly aiding and abetting others to make, use, sell, offer for sale, lease or import nonvolatile semiconductor memory products into the United States, including the Lufkin Division, that infringe one or more of the inventions covered by the claims of the '309 patent, either literally or by equivalents.

57. SanDisk's infringement of the '309 patent has been willful, and any further infringement of the '309 patent by SanDisk would be with full knowledge of Samsung's legal interest in the '309 patent and would be deliberate and willful.

COUNT FIVE
Preliminary and Permanent Injunction

58. Samsung incorporates by reference paragraphs 1 through 57 as though fully set forth herein.

59. As a consequence of SanDisk's activities described herein, Samsung has been irreparably harmed to an extent yet ascertained, and will continue to be irreparably harmed by such activities in the future unless SanDisk is enjoined by this Court from engaging in said activities. Samsung has no adequate remedy at law.

PRAYER FOR RELIEF

WHEREFORE, Samsung requests that this Court enter judgment against SanDisk and grant Samsung the following relief:

1. Issue a preliminary injunction enjoining SanDisk from any further activity that infringes on one or more claims of the following Samsung's patents:

   (a) United States Patent No. 5,473,563;
   (b) United States Patent No. 5,514,889;
   (c) United States Patent No. 5,546,341; and
   (d) United States Patent No. 5,642,309;

2. Upon final hearing, permanently enjoin SanDisk from any activity that infringes on one or more claims of the Samsung's patents;

3. Find that SanDisk's infringement of Samsung's patents was and is willful;

4. Find that this an exceptional case and award Samsung reasonable attorneys fees in accordance with 35 U.S.C. 285; and

5. Award Samsung the costs it has incurred to prosecute this action.

Dated: March 4, 2002.

Respectfully submitted,

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US005473563A

United States Patent [19]

Suh et al.

[11] **Patent Number: 5,473,563**

[45] **Date of Patent: Dec. 5, 1995**

[54] **NONVOLATILE SEMICONDUCTOR MEMORY**

[75] Inventors: **Kang D. Suh**, Ahnyang; **Jin K.S. Kim**, Seoul; **Jeong H. Choi**, Kwacheteon, all of Rep. of Korea

[73] Assignee: **Samsung Electronics Co., Ltd.**, Suwon, Rep. of Korea

[21] Appl. No.: **171,300**

[22] Filed: **Dec. 22, 1993**

[30] **Foreign Application Priority Data**

Jan. 13, 1993 [KR] Rep. of Korea 1993-390

[51] **Int. Cl.**[6] **G11C 7/00**; G11C 11/40

[52] **U.S. Cl.** **365/185.13**; 365/189.01; 365/189.05; 365/230.06

[58] **Field of Search** 365/1/185, 218, 365/900, 189.01, 189.05, 230.06

[56] **References Cited**

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5,345,418	9/1994	Challa	365/185

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"A Nand Structured Cell With A New Programmining Technology For Highly Reliable 5V-Only Flash EEPRROM", R. Kirisawa, S. Aritome, R. Nakayama, T. Endoh, R. Shirota, and F. Masuoka, 1990 Symposium on VLSI Technology.

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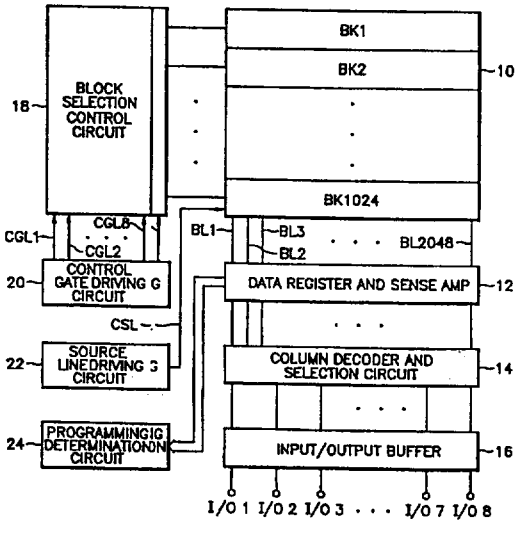
Primary Examiner—Tan T. Nguyen

Attorney, Agent, or Firm—Robert A. Westerlund; Stephen R. Whitt; Charles R. Donohoe

[57] **ABSTRACT**

A nonvolatile semiconductor memory device comprising an array of cell units, each cell unit including at least one memory transistor which has a floating gate and a control gate, the array being divided into a plurality of memory blocks each having a certain number of cell units. A selected memory block is erased by an erase voltage applied to a semiconductor substrate while unselected memory blocks are prevented from erasing by capacitive coupling of the erase voltage to floated word lines connected to control gates of memory transistors of the unselected memory blocks. In a program mode where a program voltage is applied to a selected word line of a selected memory block and a pass voltage is applied to unselected word lines of the selected memory block, channel regions and source and drain junctions of memory transistors of cell units in the selected memory block are charged to a program inhibition voltage. Channel regions and source and drain junctions of cell units associated with memory transistors programmed to the other binary data are discharged to be programmed while those of cell units associated with nonprogrammed memory transistors are maintained to the program inhibition voltage to prevent programming.

6 Claims, 19 Drawing Sheets



EXHIBIT

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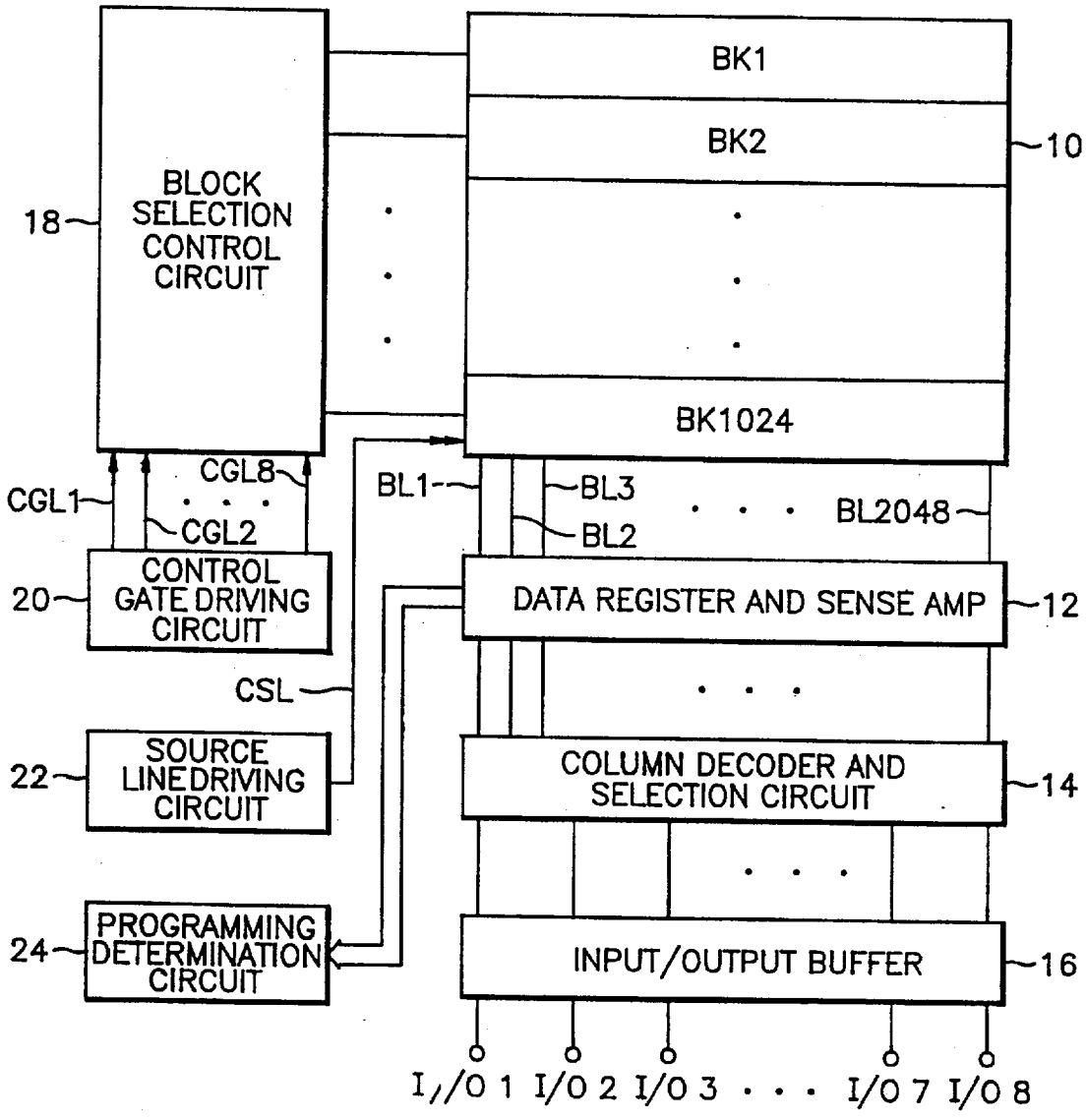
A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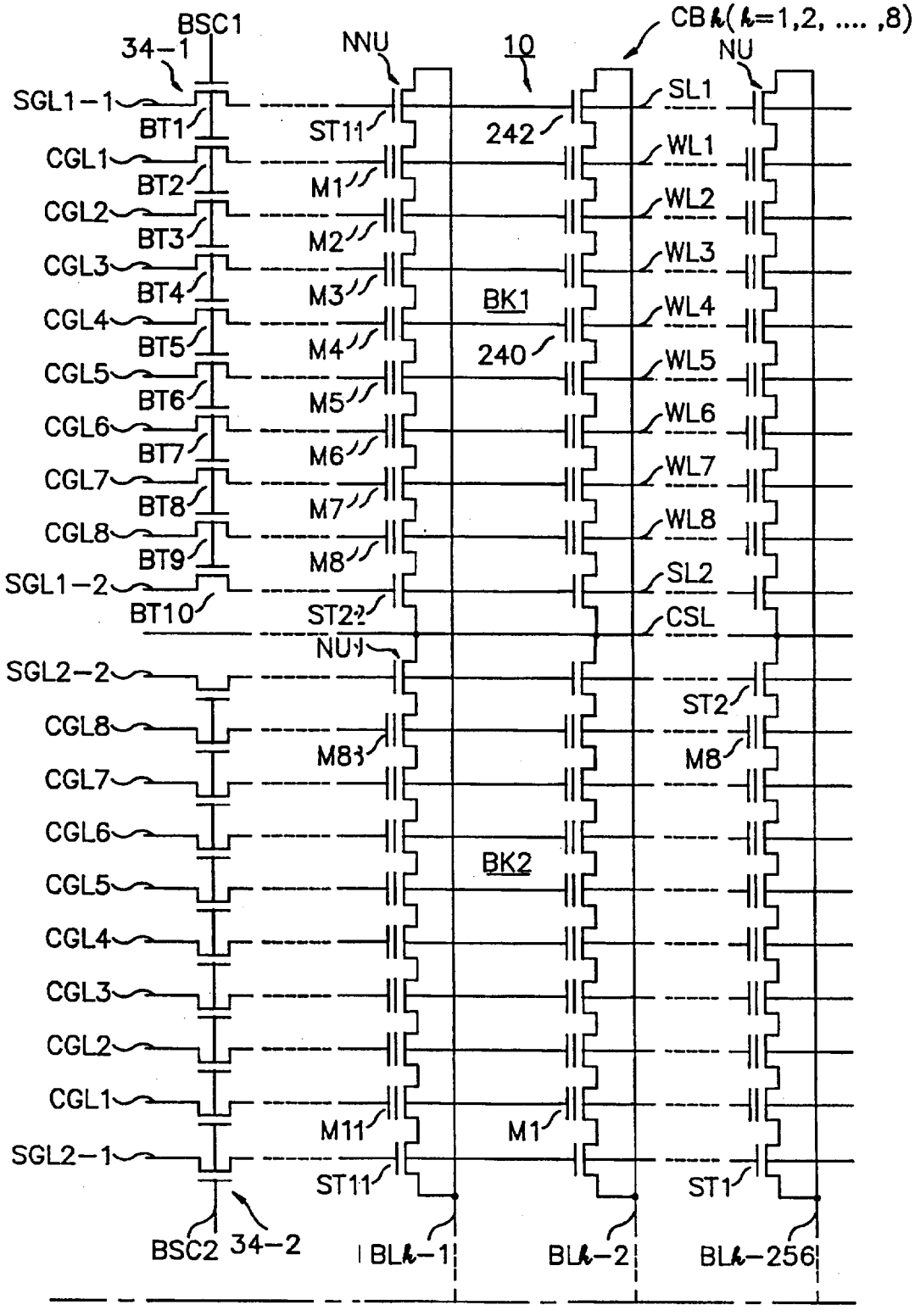
BK2
BK1024
10
BLOCK SELECTION CONTROL CIRCUIT
18
CGL1
CGL8
CGL2
BL1
BL3
BL2
BL2048
CONTROL GATE DRIVING CIRCUIT
20
DATA REGISTER AND SENSE AMP
12
CSL
SOURCE LINE DRIVING CIRCUIT
22
COLUMN DECODER AND SELECTION CIRCUIT
14
PROGRAMMING DETERMINATION CIRCUIT
24
INPUT/OUTPUT BUFFER
16
I/O 1 I/O 2 I/O 3 I/O 7 I/O 8

FIG. 1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34-1
NNU
10
CBk(k=1,2, ... ,8)
NU
SGL1-1
BT1
ST11
242
SL1
CGL1
BT2
M1
WL1
CGL2
BT3
M2
WL2
CGL3
BT4
M3
WL3
CGL4
BT5
M4
BK1
WL4
CGL5
BT6
M5
240
WL5
CGL6
BT7
M6
WL6
CGL7
BT8
M7
WL7
CGL8
BT9
M8
WL8
SGL1-2
BT10
ST22
SL2
NU1
CSL
SGL2-2
CGL8
M83
ST2
CGL7
M8
CGL6
CGL5
BK2
CGL4
CGL3
CGL2
CGL1
M11
M1
SGL2-1
ST11
ST1
BSC2
34-2
BLk-1
BLk-2
BLk-256

FIG. 2a

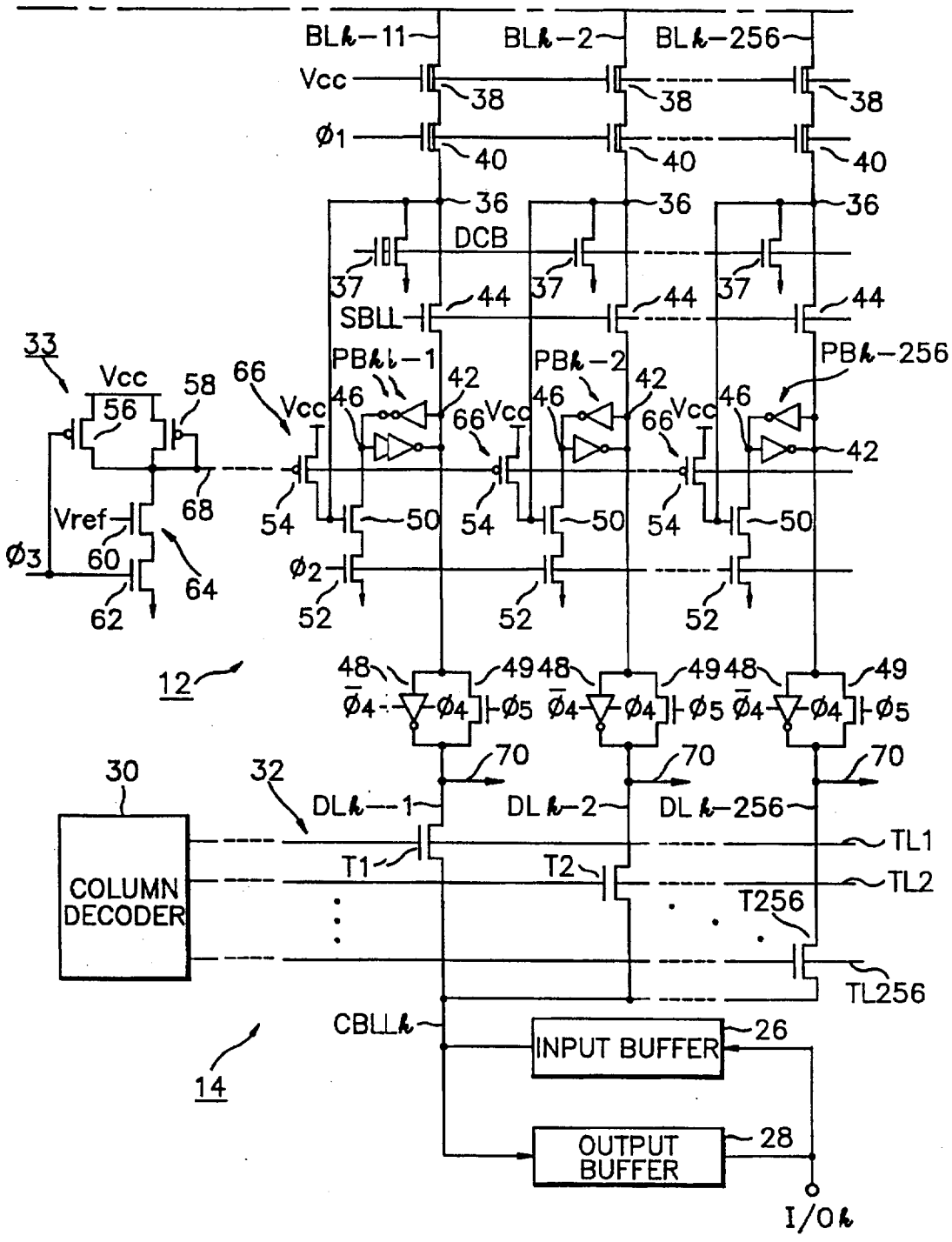

BLk-11
BLk-2
BLk-256
Vcc
Ø1
38
40
36
DCB
37
44
SBLL
33
PBk-1
PBk-2
PBk-256
Vcc
58
56
66
46
42
Vref
68
60
64
62
54
50
Ø3
Ø2
52
12
48
49
Ø4
Ø5
70
30
32
DLk-1
DLk-2
DLk-256
COLUMN DECODER
T1
T2
T256
TL1
TL2
TL256
CBLLk
INPUT BUFFER
26
OUTPUT BUFFER
28
I/Ok
14

FIG. 2b

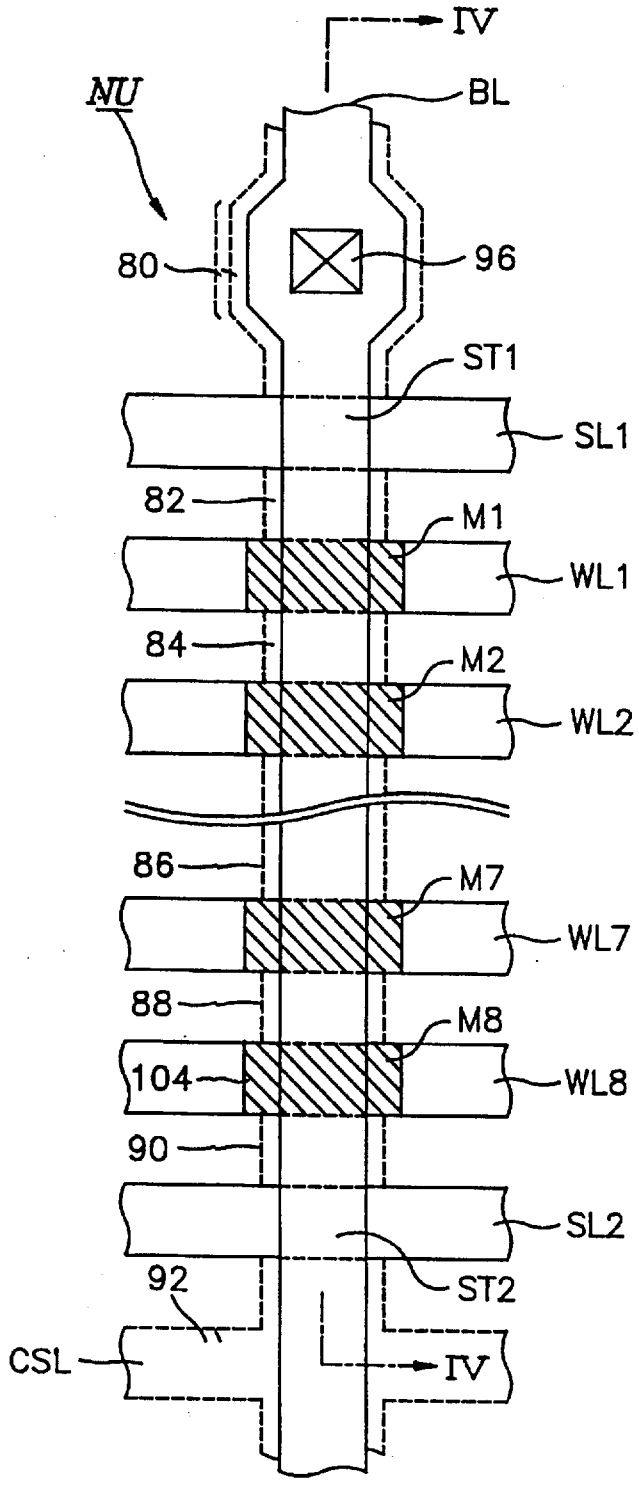
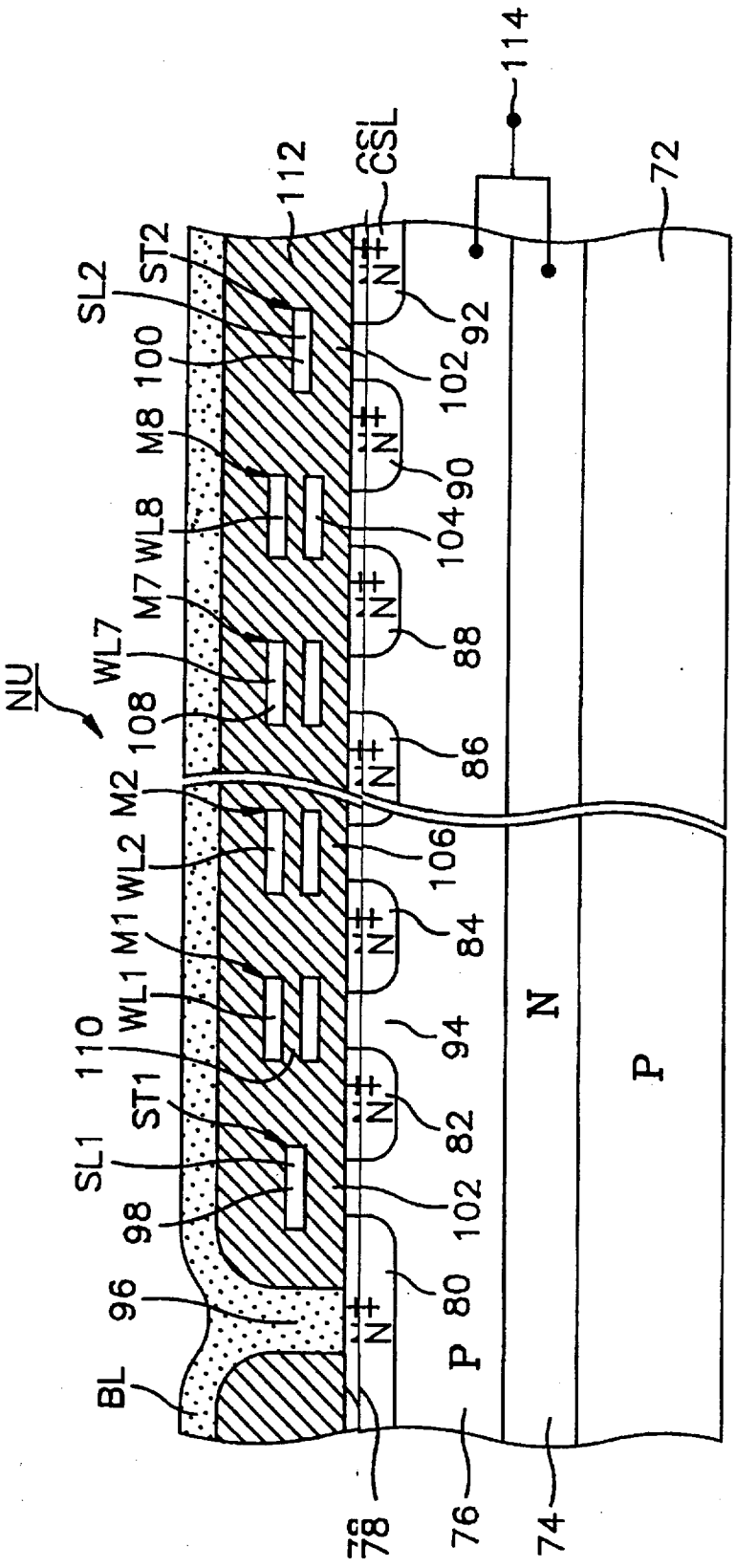

IV
NU
BL
80
96
ST1
SL1
82
M1
WL1
84
M2
WL2
86
M7
WL7
88
M8
104
WL8
90
SL2
92
ST2
CSL
IV

FIG. 3


114
112
CSL
72
SL2
ST2
100
M8
WL8
M7
WL7
NU
108
M2
WL2
M1
WL1
110
ST1
SL1
98
96
BL
92
102
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104
88
86
106
84
94
82
102
80
N+
N
P
78
76
74

FIG. 4

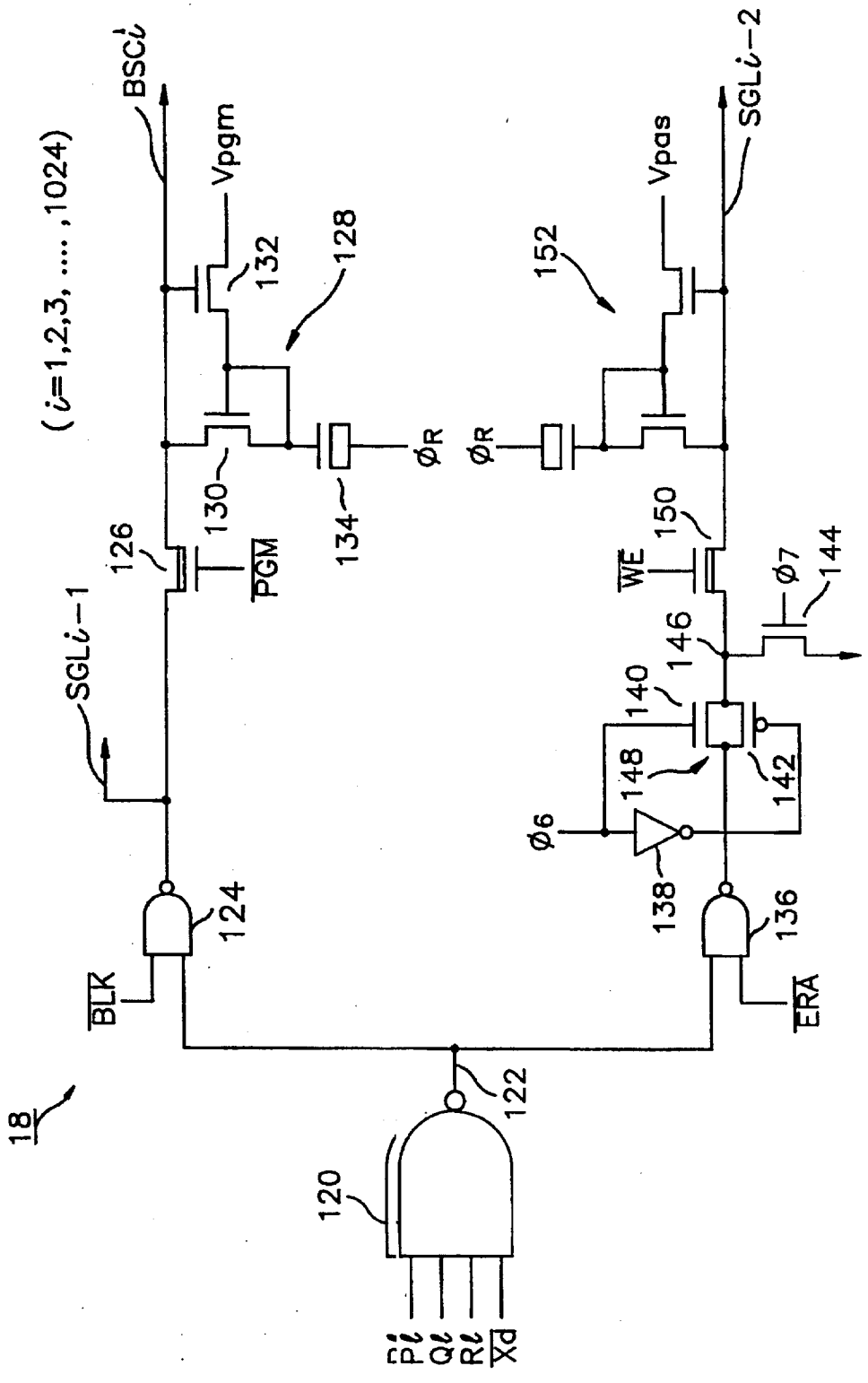
BSCi
Vpgm
132
128
152
Vpas
SGLi-2
(i=1,2,3, ... ,1024)
ØR
ØR
130
134
126
PGM
150
WE
144
Ø7
SGLi-1
146
140
148
142
Ø6
138
124
136
BLK
ERA
18
122
120
Pi
Qi
Ri
Xd

FIG. 5

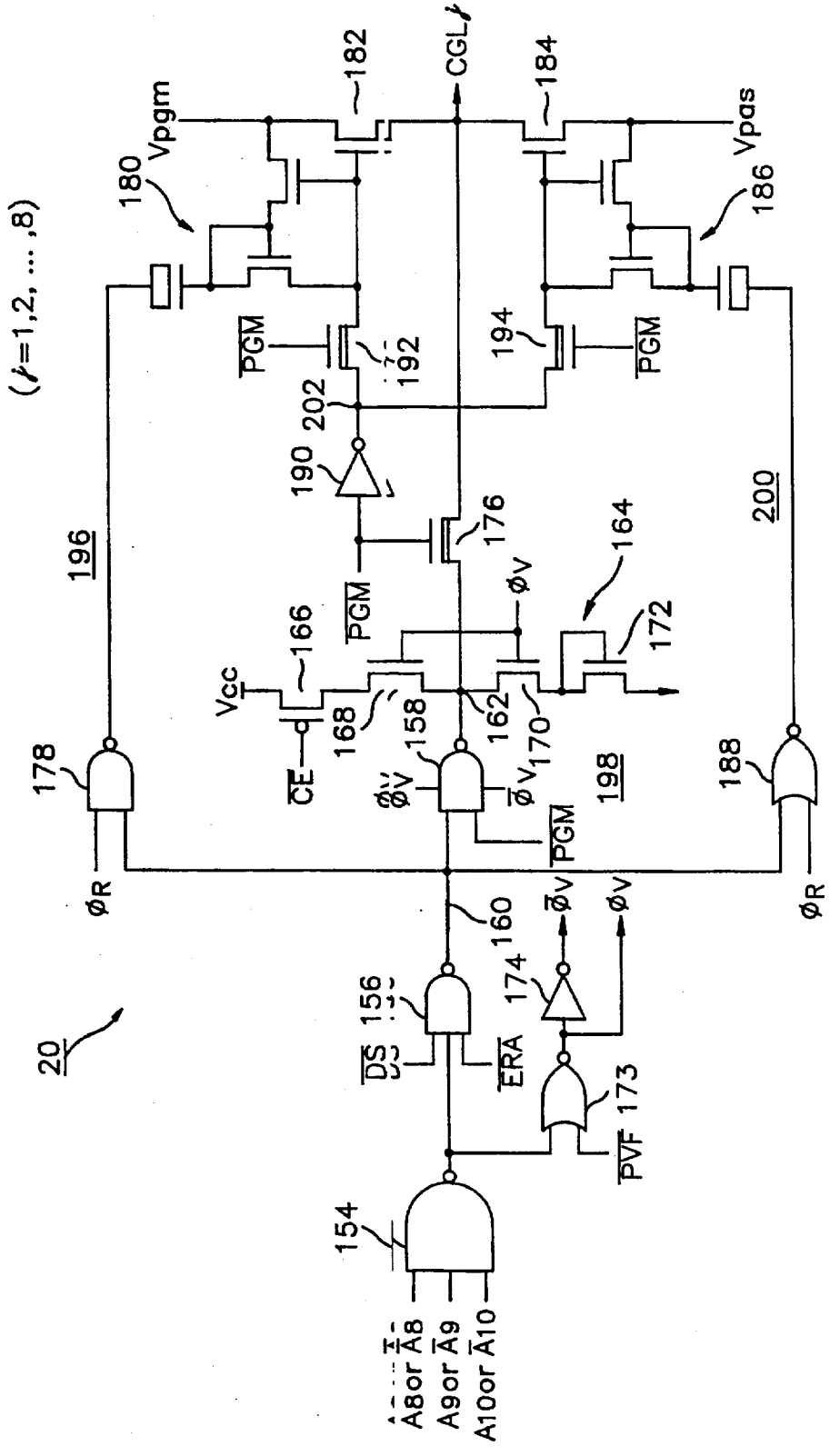
(ℓ=1,2, ... ,8)
Vpgm
Vpas
CGLℓ
180
182
184
186
PGM
192
194
202
190
176
164
196
200
166
172
Vcc
168
158
162
170
178
188
CE
198
ØR
160
174
156
173
20
ERA
PVF
154
A8 or Ā8
A9 or Ā9
A10 or Ā10

FIG. 6

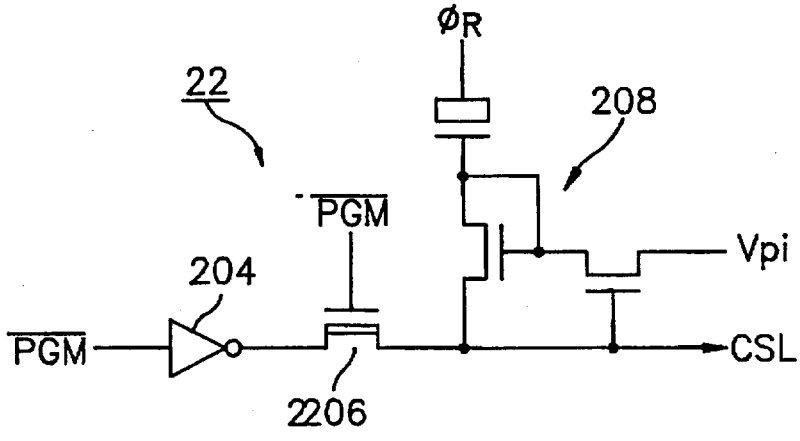

FIG. 7

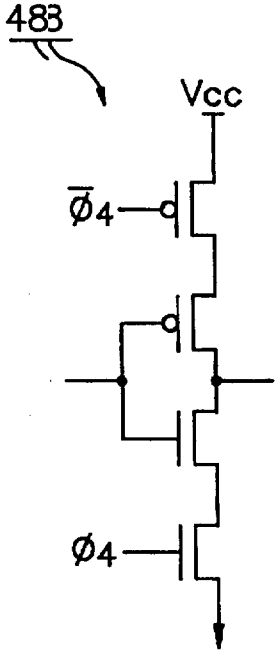

FIG. 8a

FIG. 8

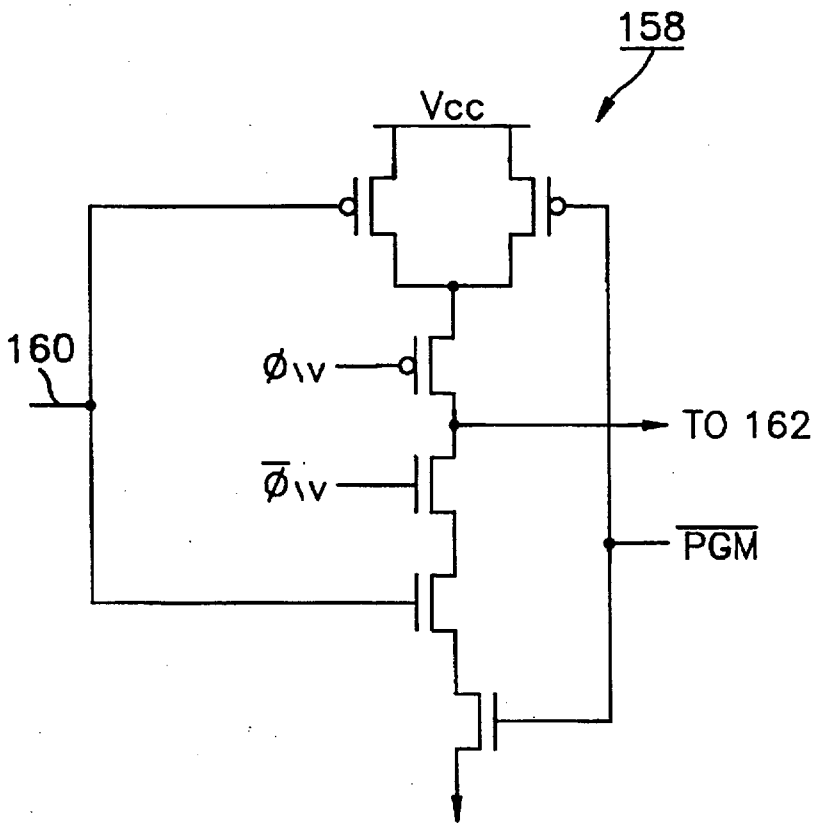
158
Vcc
160
ϕ_{1V}
$\overline{\phi}_{1V}$
TO 162
$\overline{PGM}$

FIG. 8b

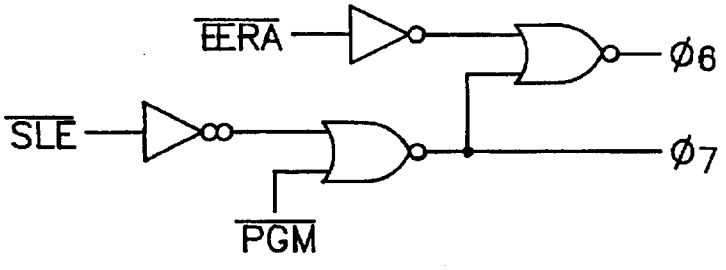
$\overline{EERA}$
$\overline{SLE}$
$\overline{PGM}$
ϕ_6
ϕ_7

FIG. 8c

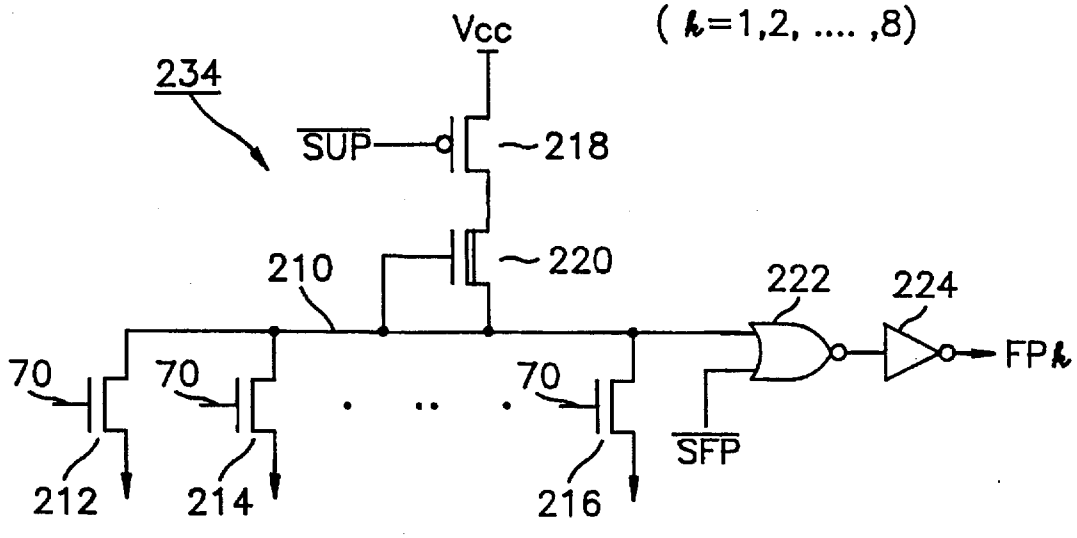

FIG. 9a

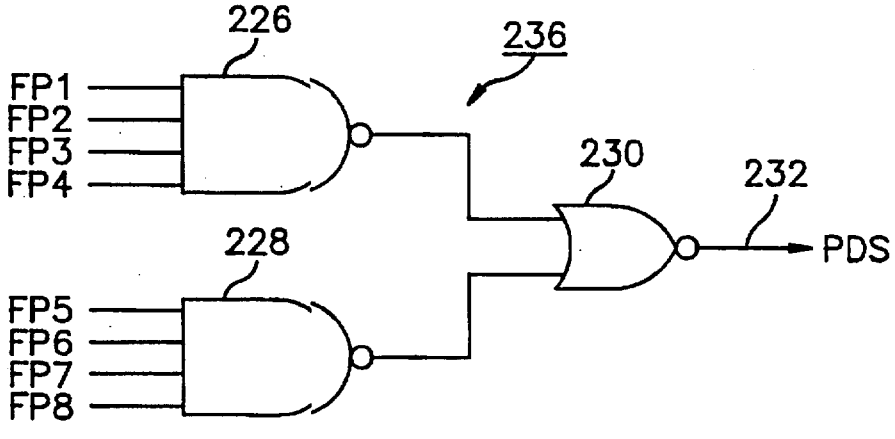

FIG. 9b

FIG. 9

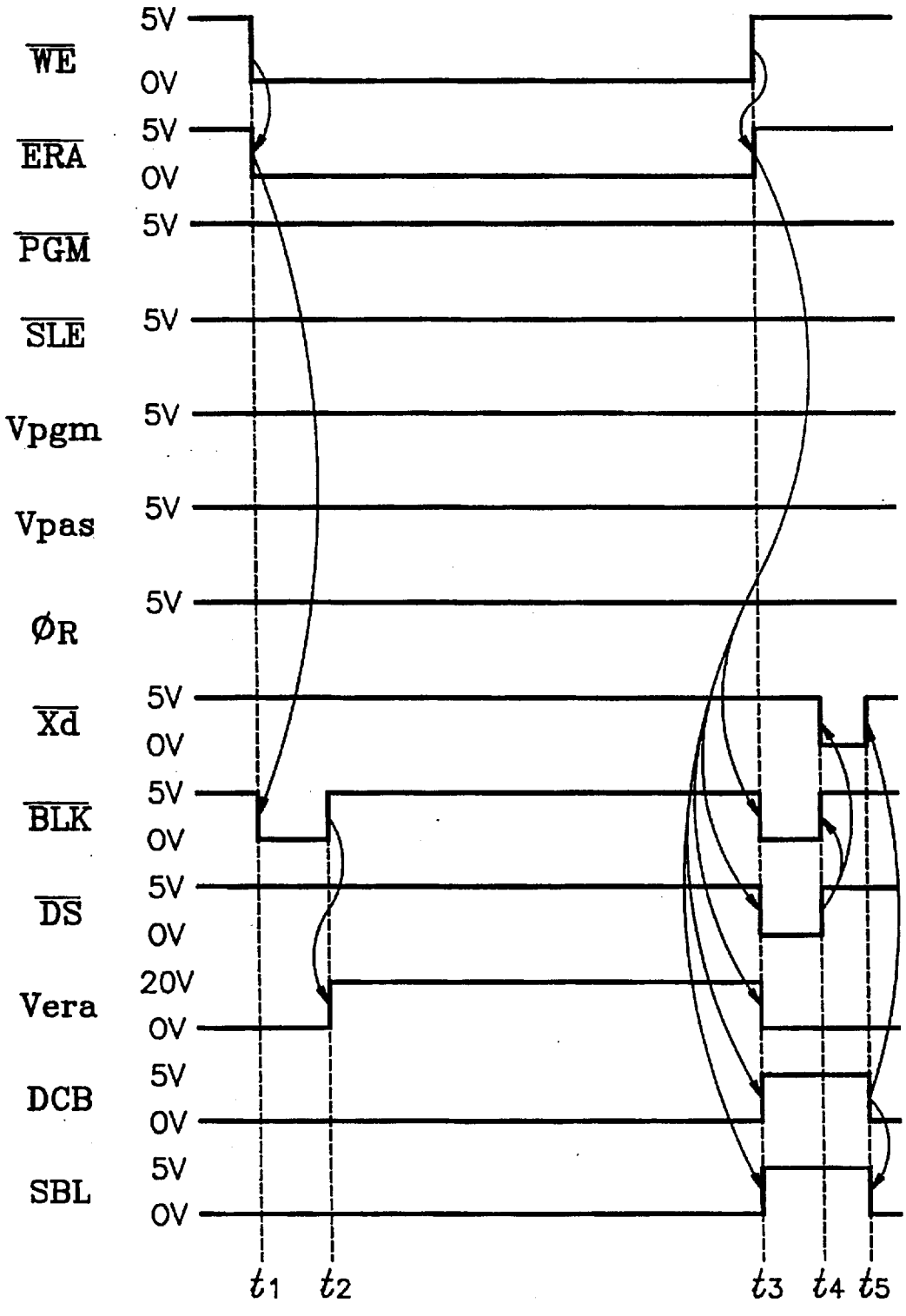
WE
ERA
PGM
SLE
Vpgm
Vpas
ØR
Xd
BLK
DS
Vera
DCB
SBL
5V
0V
20V
t1
t2
t3
t4
t5

FIG. 10

US005514889A

United States Patent [19]

Cho et al.

[11] Patent Number: 5,514,889

[45] Date of Patent: May 7, 1996

[54] **NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME**

[75] Inventors: **Myoung-kwan Cho; Jeoug-hyyuk Choi**, both of Kyungki, Rep. of Koreæa

[73] Assignee: **Samsung Electronics Co., Ltdd.**, Suwon, Rep. of Korea

[21] Appl. No.: **107,901**

[22] Filed: **Aug. 18, 1993**

[30] **Foreign Application Priority Data**

Aug. 18, 1993 [KR] Rep. of Korea 14810/92

[51] **Int. Cl.**[6] **H01L 29/788**

[52] **U.S. Cl.** ..... **257/316**; 257/371; .; 257/548; 257/324

[58] **Field of Search** 257/316, 371, 257/548, 324

[56] **References Cited**

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5,063,431	11/1991	Ohshima	257/316
5,341,342	8/1994	Brahmbhatt	257/316

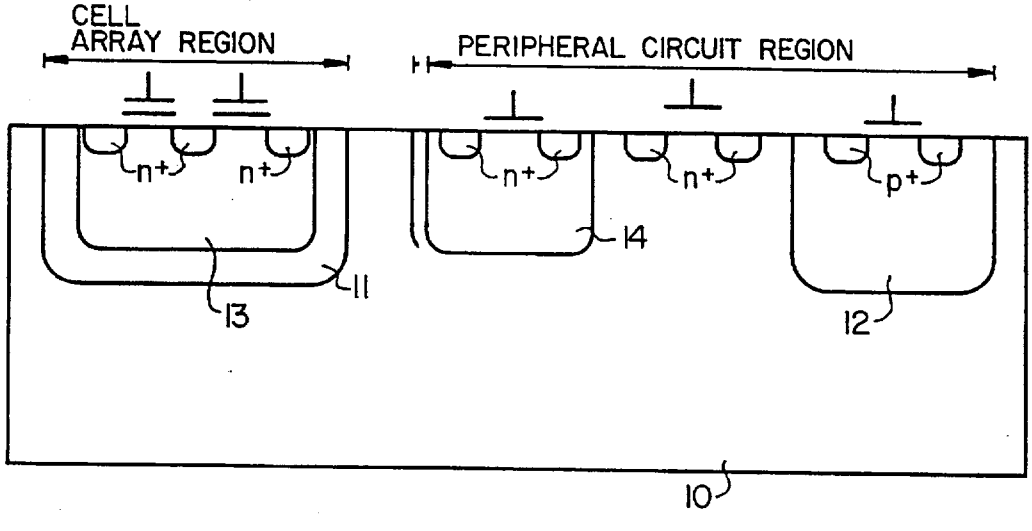
Primary Examiner—Edward Wojciechowicz

Attorney, Agent, or Firm—Cushman Darby & Cushman

[57] **ABSTRACT**

An EEPROM device in which a high voltage is applied to the chip during the memory cell operation and a method for the manufacturing the same are disclosed. On a P-type semiconductor substrate, a first N-well is formed in a surface portion of the substrate in the cell array region and a second N-well is formed in a first surface of the substrate in the peripheral circuit region. An EEPROM memory cell is formed on the first P-well and a first NMOS transistor is formed on the second P-well. Also, a second NMOS transistor is formed on a second surface portion of the semiconductor substrate in the peripheral circuit 10 region and a PMOS transistor is formed on the second N-well. The impurity concentrations of the first and second P-wells are controlled in accordance with the characteristic of the MOS transistors to be formed. Further, a second NMOS transistor having a resistance against a high voltage is directly formed on the P-type substrate. Thus, the electric characteristic of the EEPROM device is enhanced.

9 Claims, 11 Drawing Sheets



EXHIBIT

tabbies

B

FIG. 1

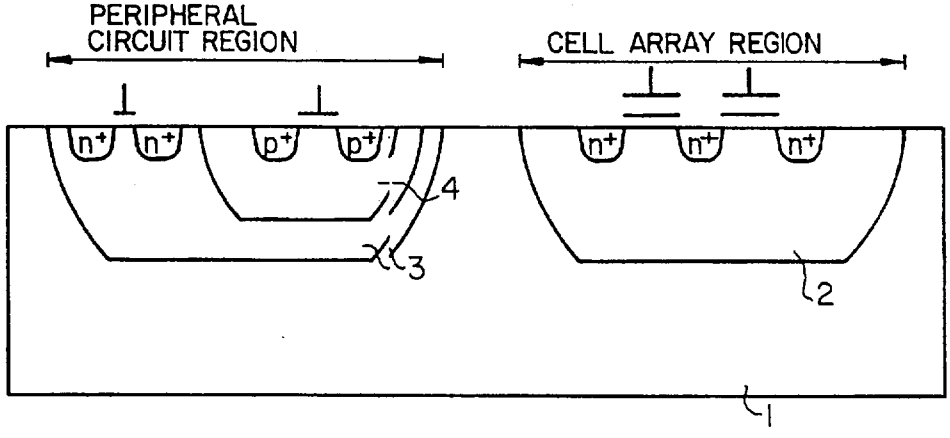
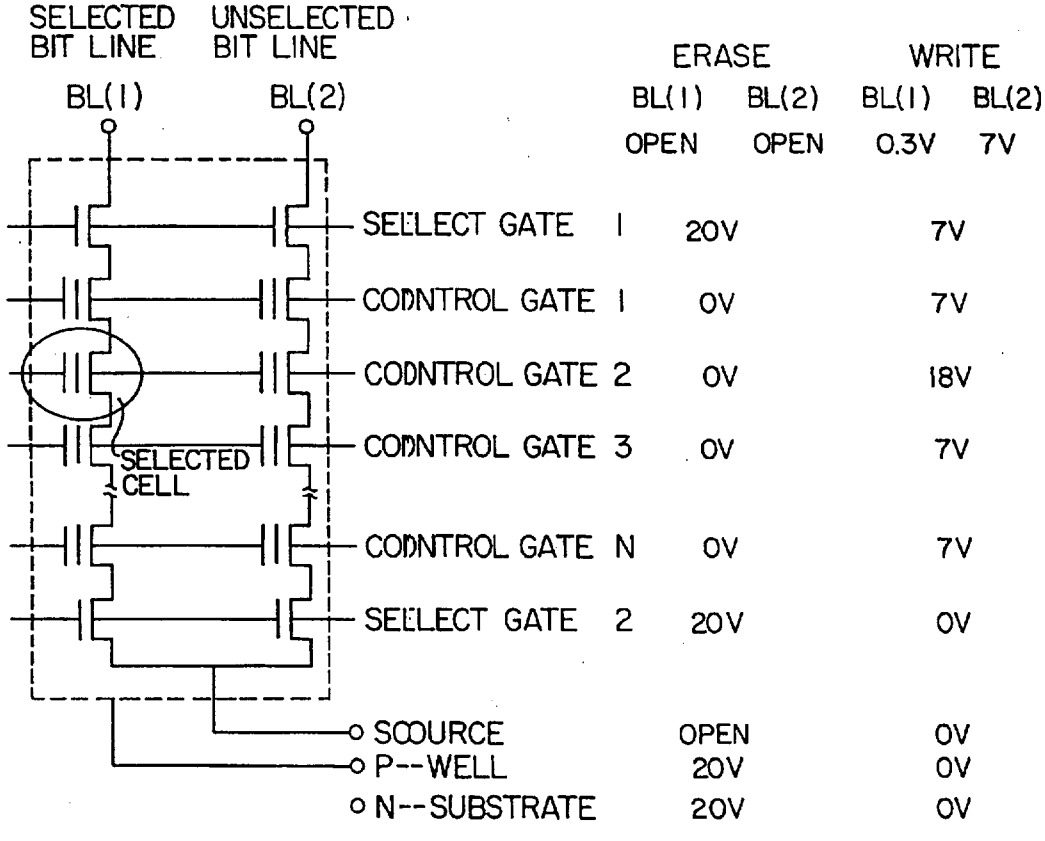
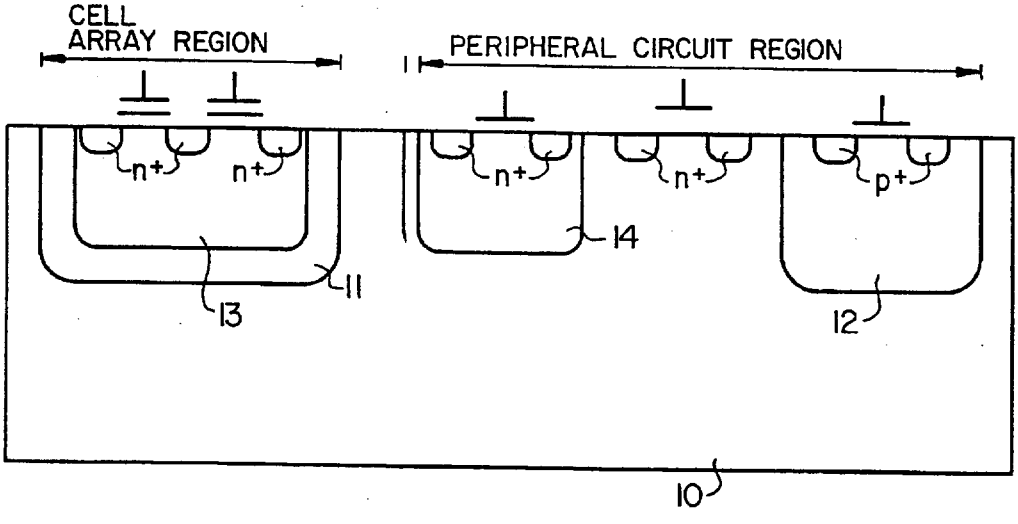


FIG. 2



	ERASE		WRITE	
	BL(1)	BL(2)	BL(1)	BL(2)
	OPEN	OPEN	0.3V	7V
SELECT GATE 1	20V		7V	
CONTROL GATE 1	0V		7V	
CONTROL GATE 2	0V		18V	
CONTROL GATE 3	0V		7V	
CONTROL GATE N	0V		7V	
SELECT GATE 2	20V		0V	
SOURCE	OPEN		0V	
P--WELL	20V		0V	
N--SUBSTRATE	20V		0V	

FIG. 3


CELL
ARRAY REGION
PERIPHERAL CIRCUIT REGION
n+
n+
n+
n+
p+
11
12
13
14
10

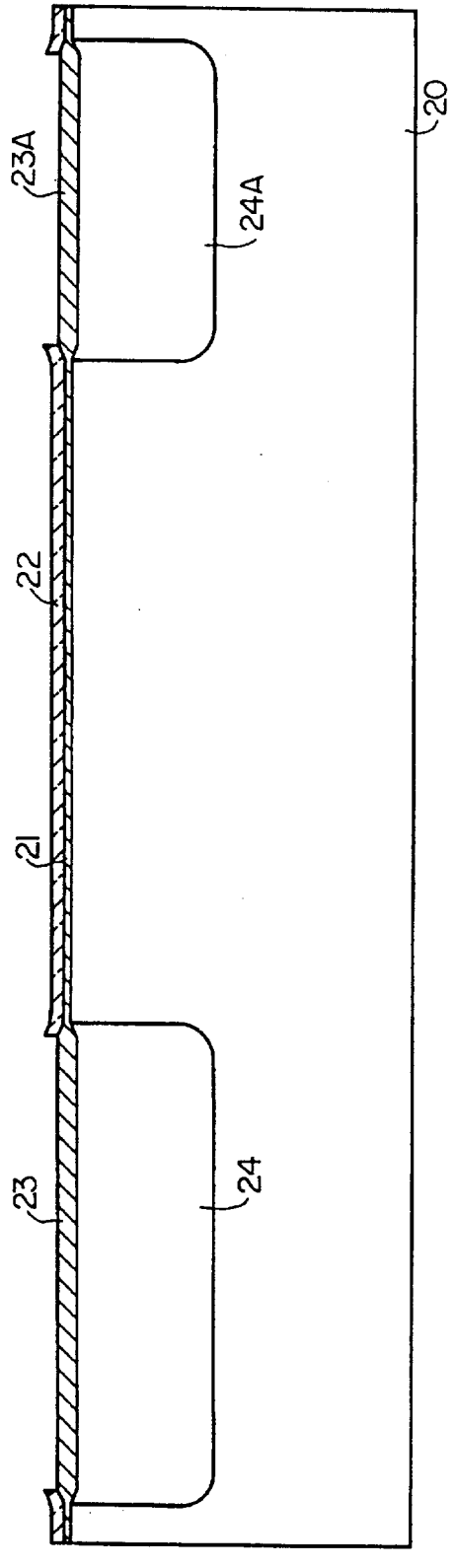


FIG. 4

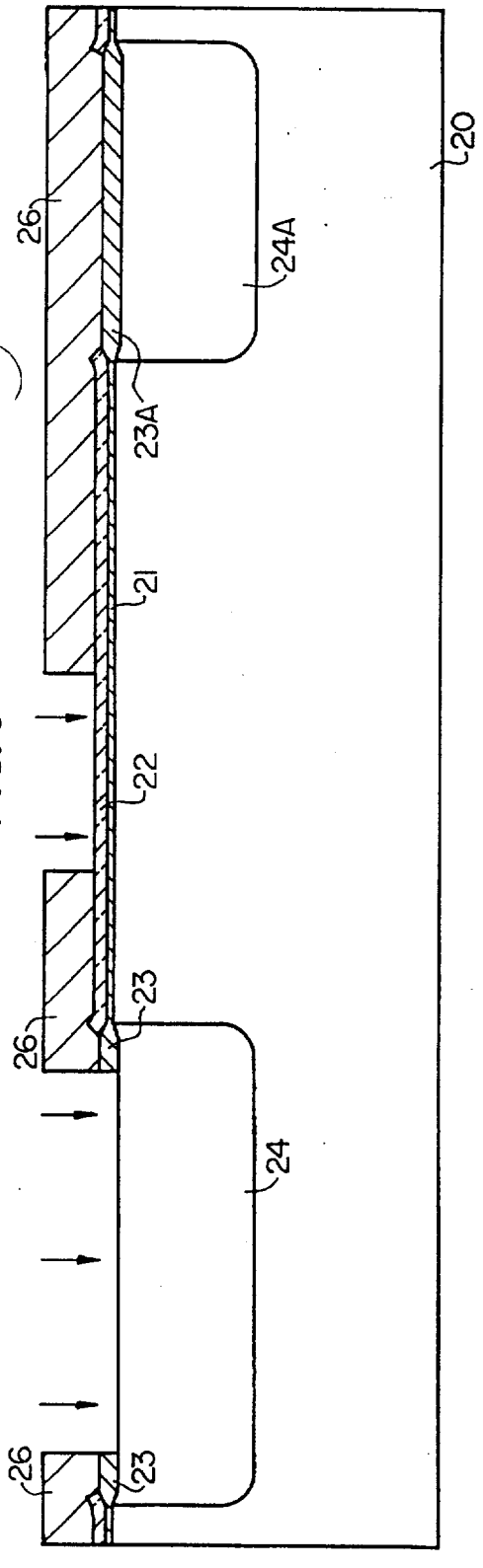


FIG. 5

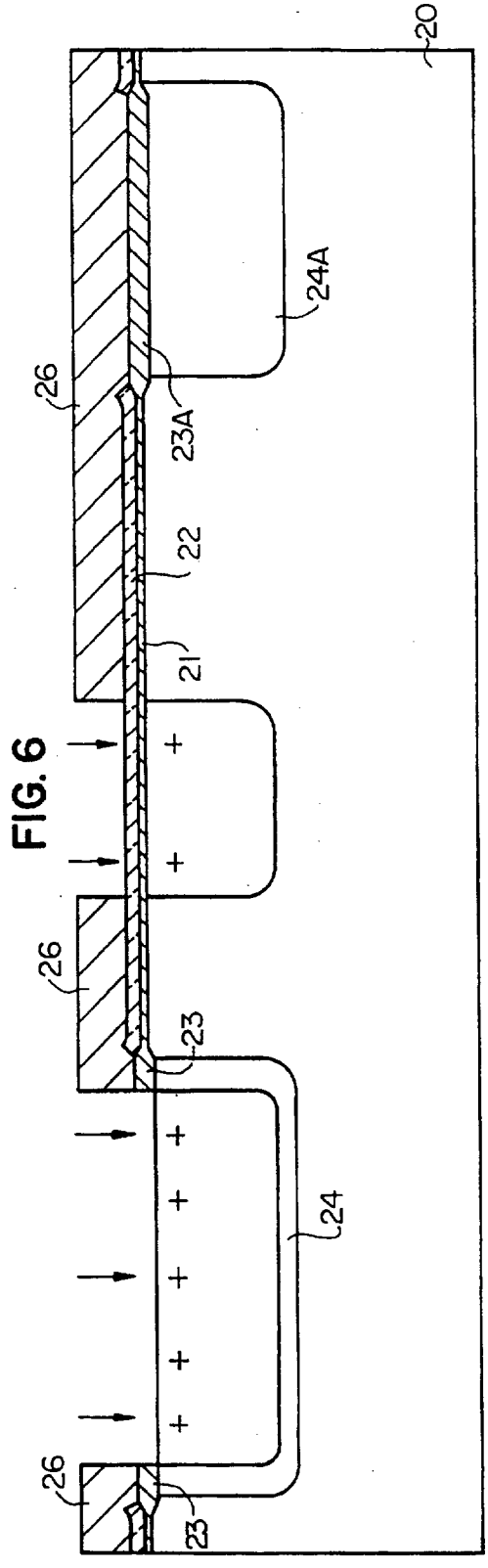

20
24A
26
23A
22
21
26
23
24
26
23

FIG. 6

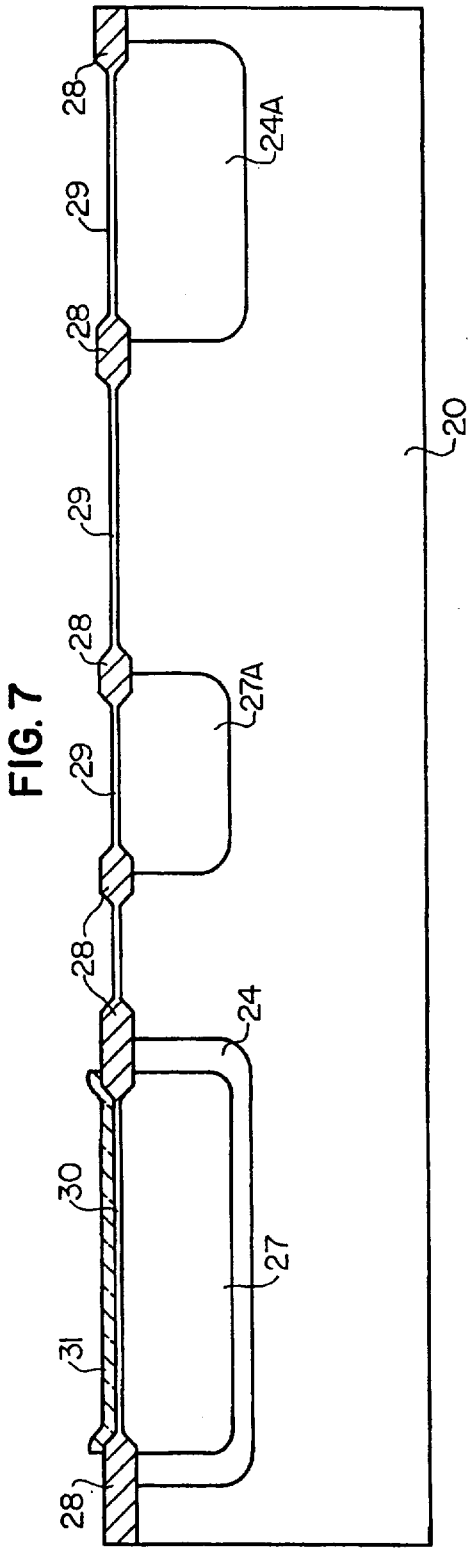

28
24A
29
28
20
29
28
27A
29
28
24
30
27
31
28

FIG. 7

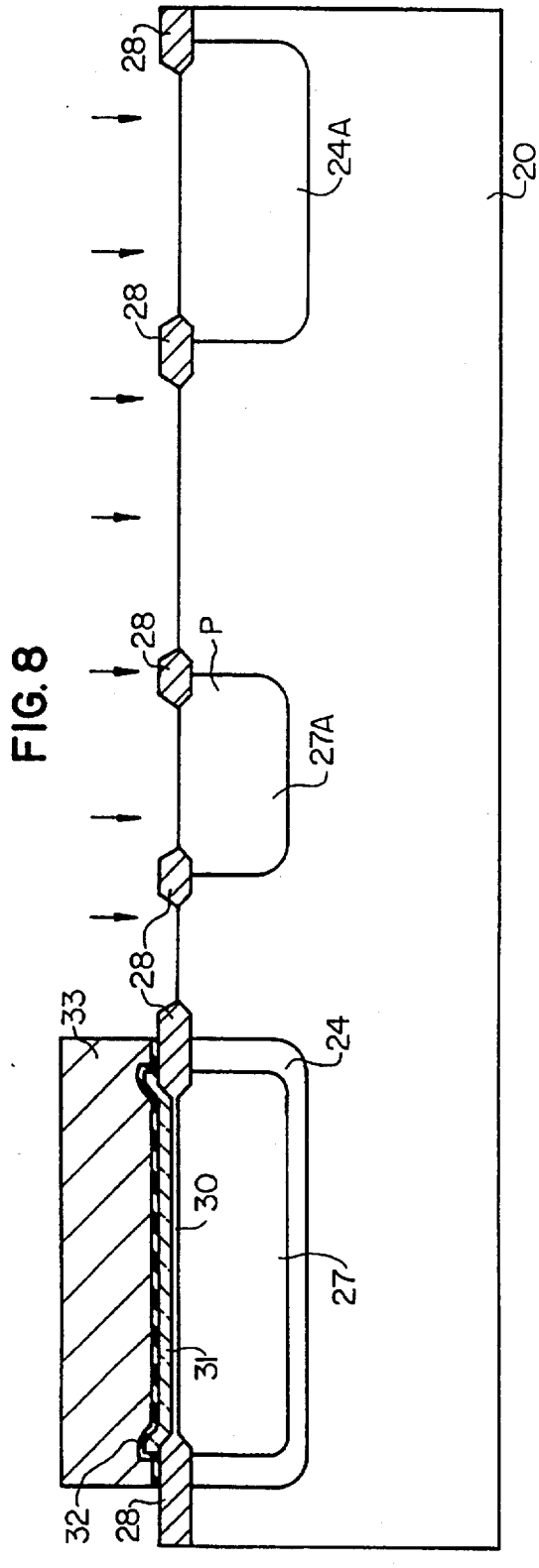

28
24A
20
28
28
P
27A
28
33
24
30
27
31
32
28

FIG. 8

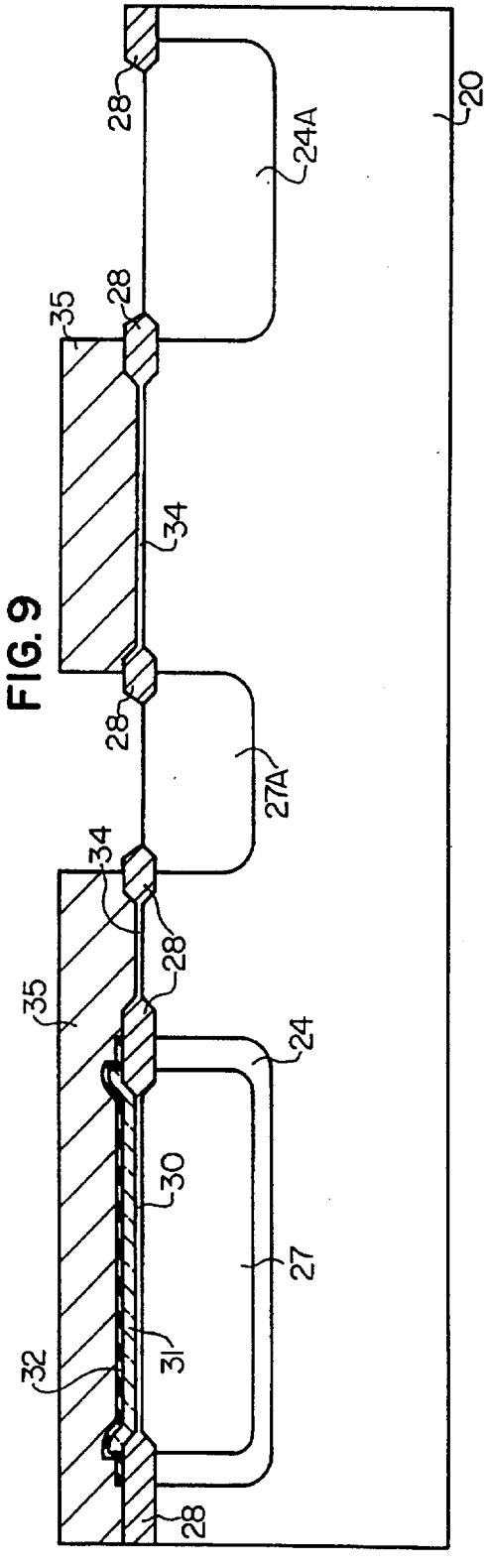

28
24A
20
35
28
34
28
27A
34
28
35
24
30
27
32
31
28

FIG. 9

FIG. 10

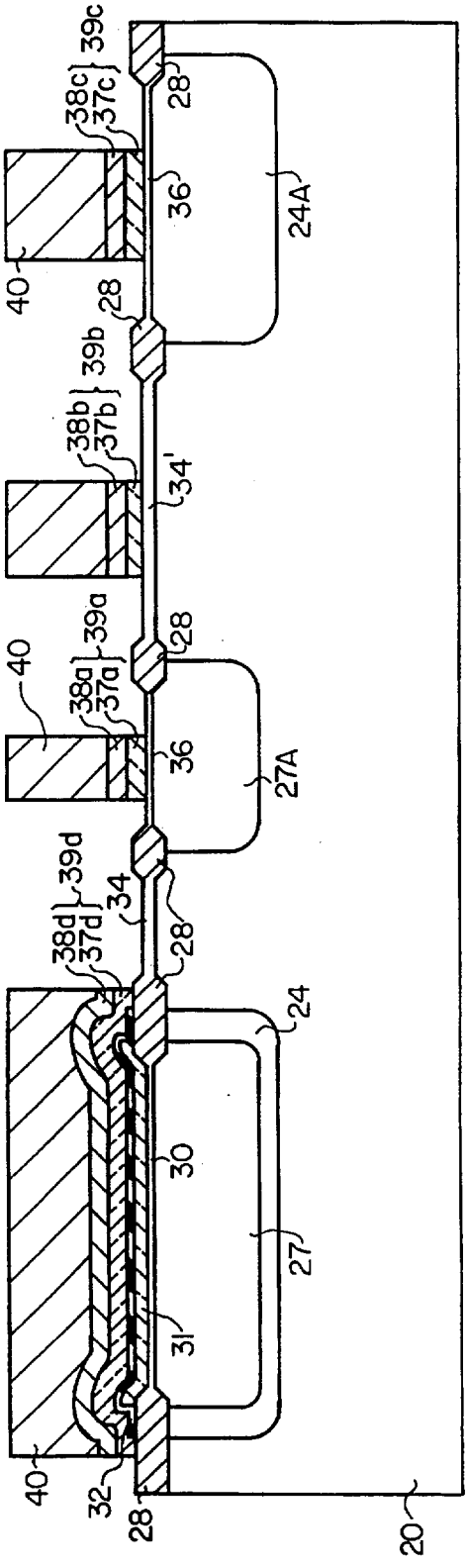
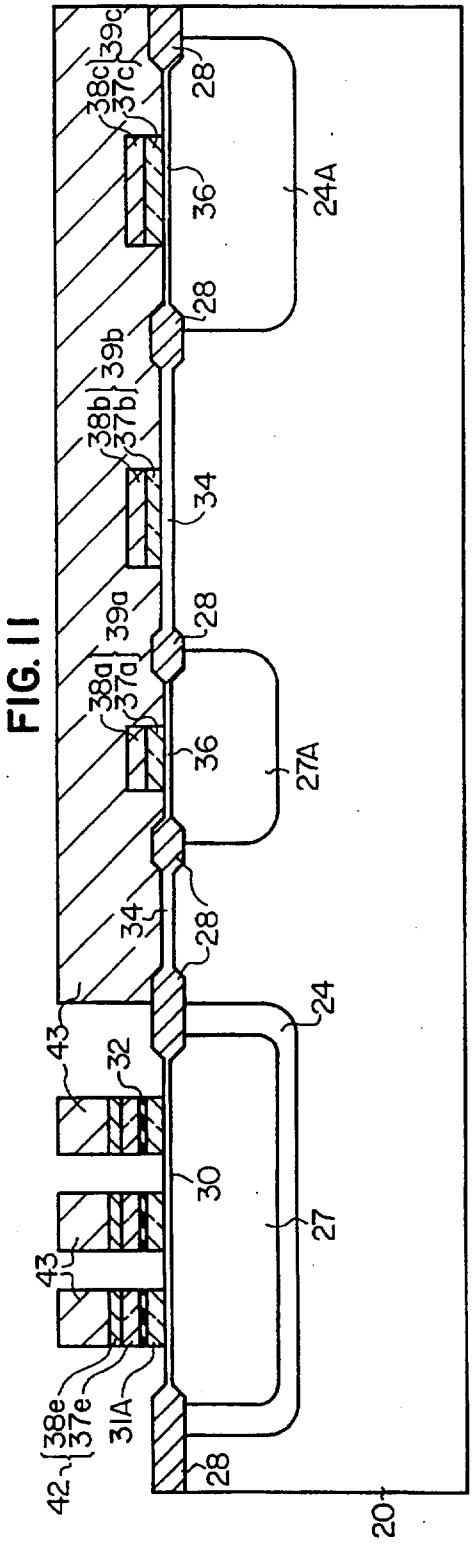

39c
38c
37c
28
36
24A
40
28
39b
38b
37b
34'
39a
38a
37a
28
40
36
27A
39d
38d
37d
34
28
24
30
27
31
40
32
28
20

FIG. 11


39c
38c
37c
28
36
24A
28
39b
38b
37b
34
39a
28
38a
37a
36
27A
34
28
24
43
32
30
27
43
38e
37e
31A
42
28
20

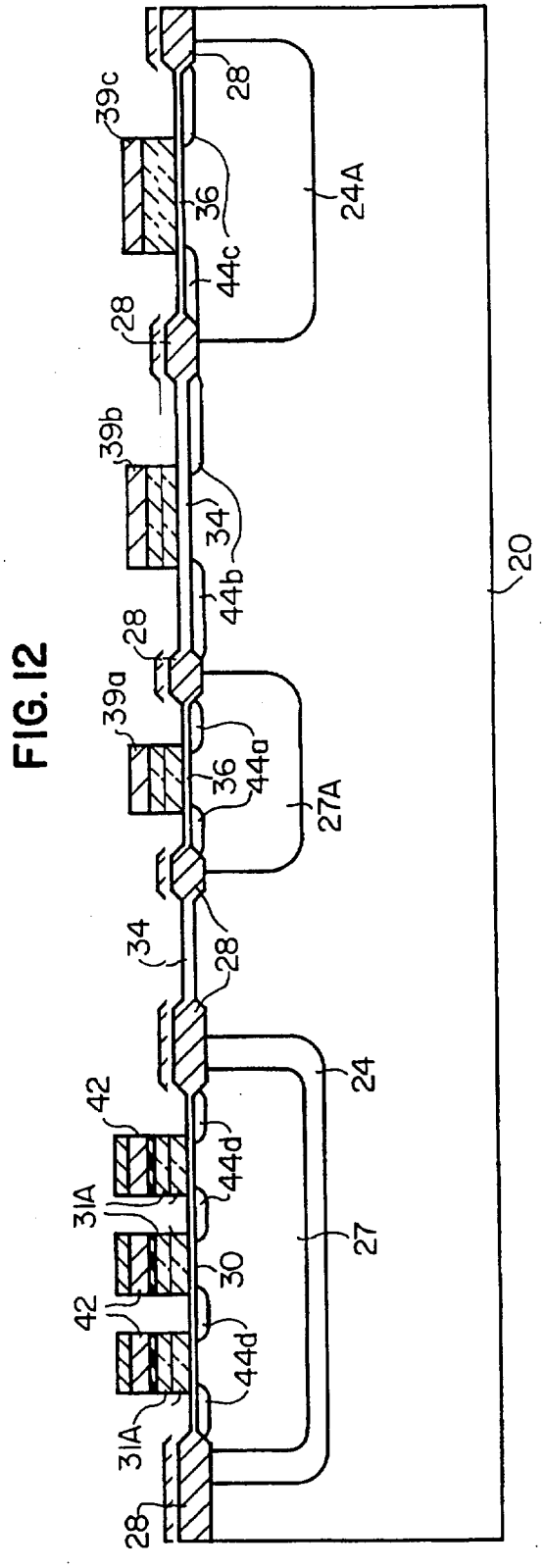

39c
28
36
24A
44c
28
39b
34
44b
28
39a
36
44a
27A
34
28
24
42
44d
31A
30
27
42
44d
31A
28
20

FIG. 12

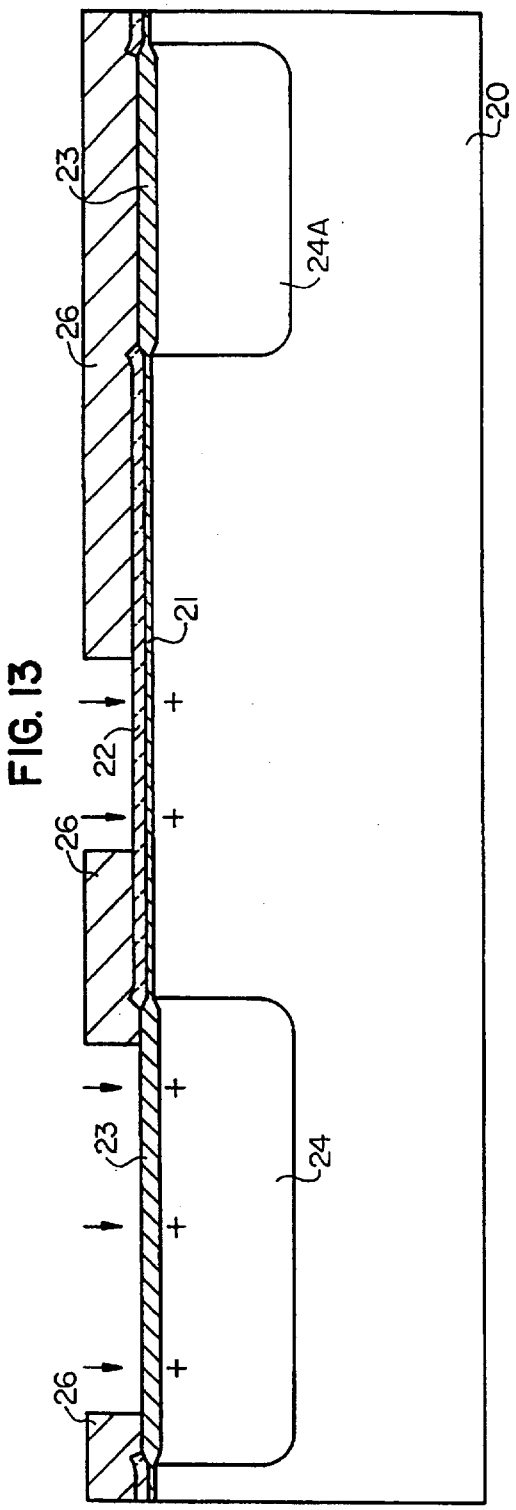


FIG. 13

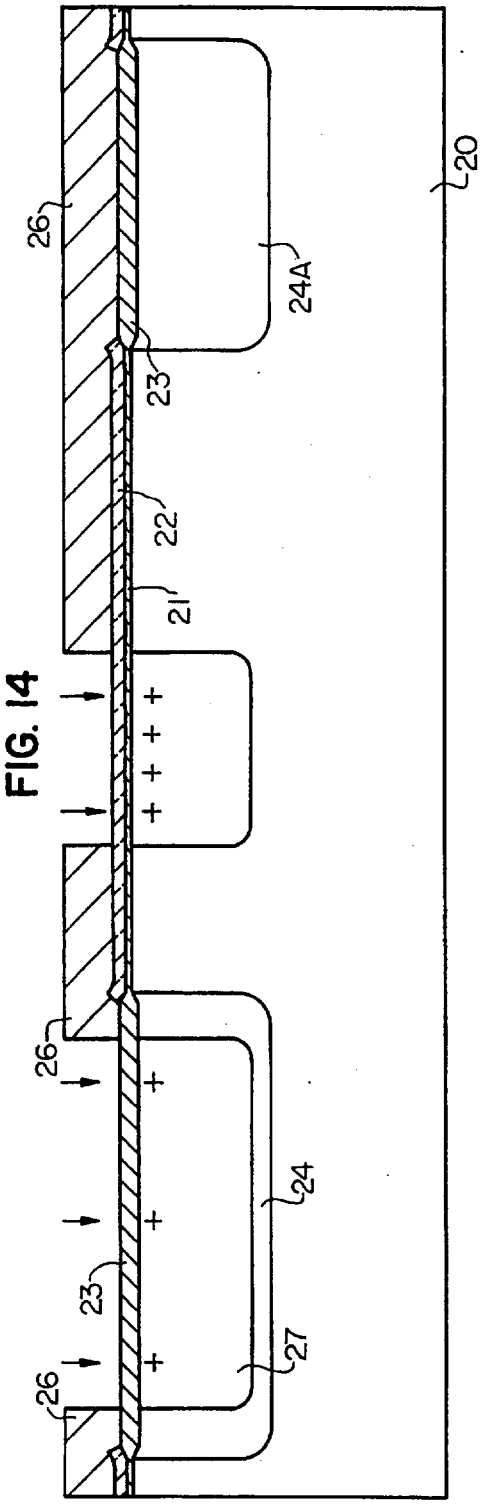


FIG. 14

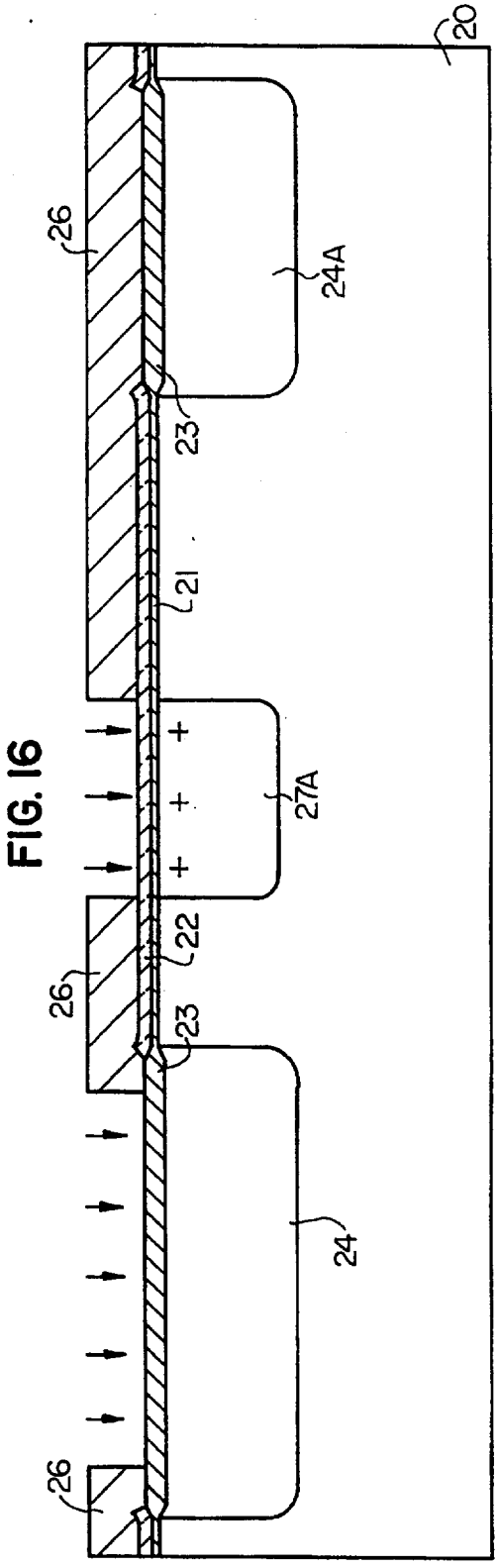

20
26
24A
23
21
27A
22
26
23
24
26

FIG. 16

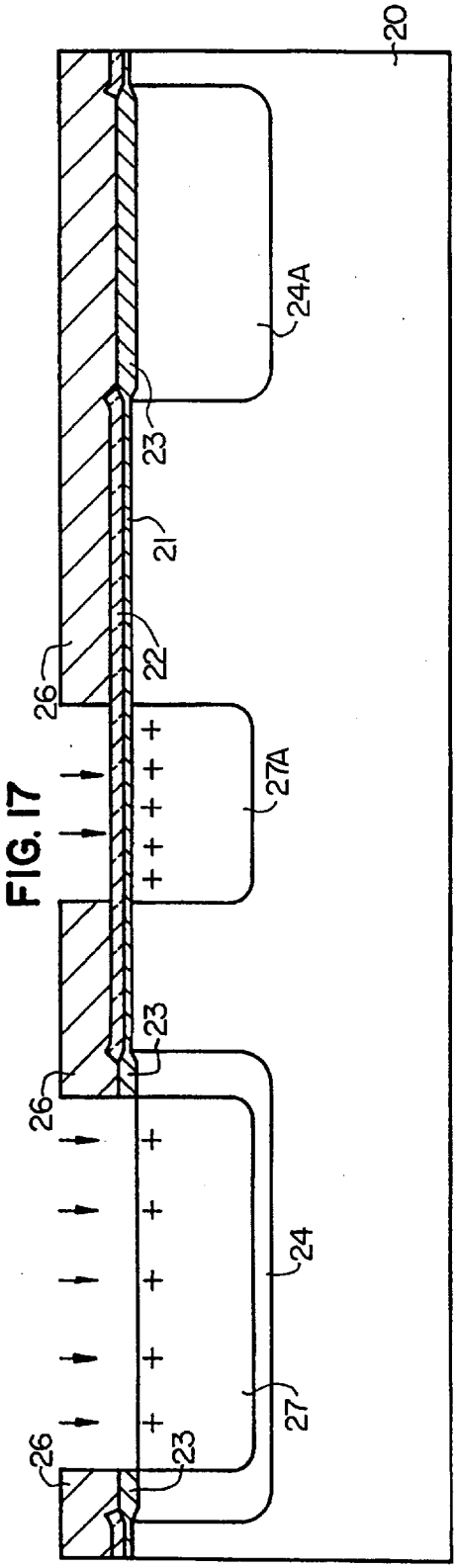

20
24A
23
21
22
26
27A
23
26
24
27
26
23

FIG. 17

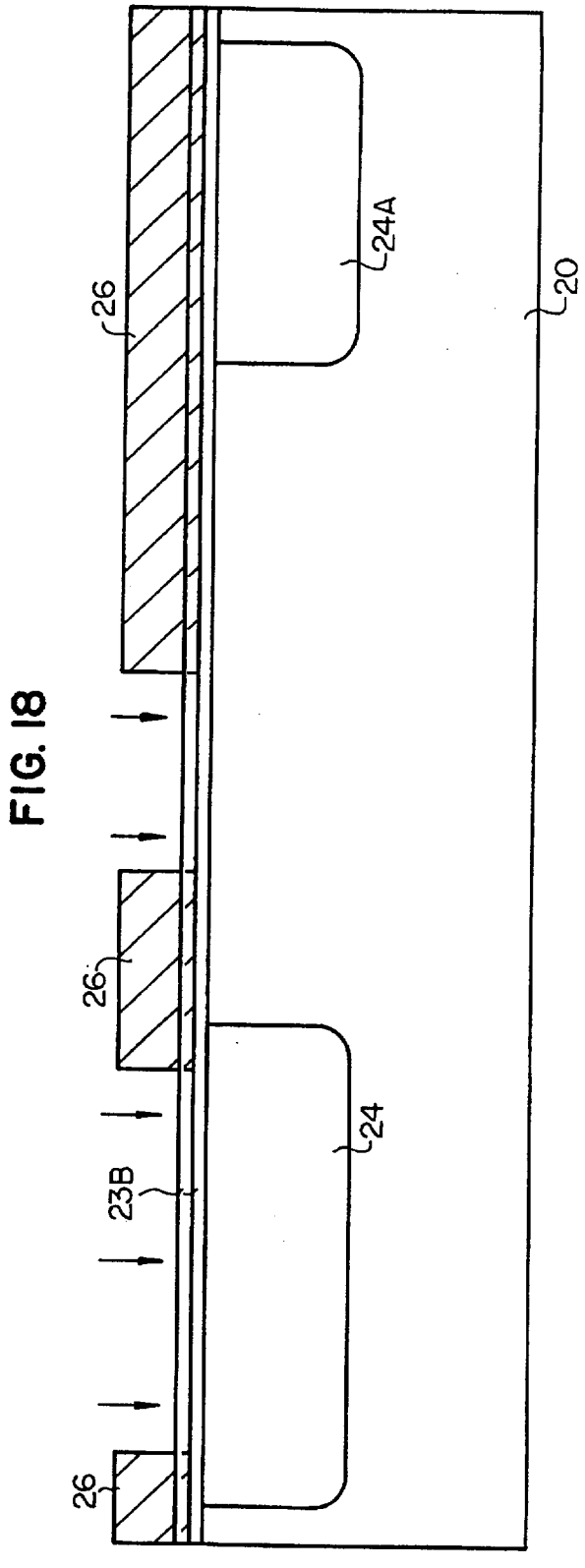


FIG. 18

NON-VOLATILE SEMICONDUCTODR MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTIONN

The present invention relates to an electricallyly erasable and programmable read only memory (EEPROM)I) device as a non-volatile semiconductor memory device and d a method for manufacturing the same, and, more particulalarly, to an EEPROM device in which a high voltage is applplied to the chip during memory cell operation and a methcod for the manufacturing the same.

Along with the progress of computer systems, thhe need for large-capacity non-volatile memories adaptable e to high-speed operation, such as memory cards, has i increased. Among these non-volatile memories, there hasis been an increased need for EEPROMs comprised of a floaating gate and a control gate and which can electrically (erase and program data. Therefore, a variety of cell struuctures for EEPROMs have been suggested for providing hiighher integration density, larger capacity and faster perforrmance.

A NAND-structured memory cell has been devveloped in order to achieve cell area reduction without streressing the fabrication technology. An advanced NAND structtured flash EEPROM has been suggested (see "A 2.3 um^2 Meemory Cell Structure For NAND EEPROMs" by R. Shirota et a al. IEDM, 1990, pp 103–106).

FIG.1 is a sectional view illustrating the abovve NAND-structured EEPROM which is manufactured asas follows. First, a first P-well 2 (in a cell array region) andd a second P-well 3 (in a peripheral circuit region) are formmed in the upper portion of an N-type semiconductor substratate 1. Then, a cell array comprised of an EEPROM is formeed on first P-well 2, an NMOS transistor of the peripheral d circuit is formed on a portion of second P-well 3, and an N-well 4 on which a PMOS transistor of the peripheral circuiuit is to be formed, is formed in a portion of second P-well 33. In order to manufacture the above EEPROM, ions are i implanted three times for forming three impurity-doped reregions (or bulks): one for forming first P-well 2 on which the e cell array is to be formed, one for forming second P-well 3 3 on which the NMOS transistor of the peripheral circuit is fooormed, and one for forming N-well 4 on which PMOS transisistor of the peripheral circuit is formed.

FIG. 2 shows a portion of an equivalent circuit ddiagram of an EEPROM device using the aforementioned conventional EEPROM cell and an erase and write (or programm) operation. The program operation of a selected cell, is ccarried out by charging electrons into the floating gate and rraising the cell's threshold voltage. This is accomplished by y applying 0.3 V to a selected bit line BL(1) of the cell arrayy and 7 V to an unselected bit line BL(2) of the cell array as a a program preventing voltage, and applying 10 V to the uunselected control gate and 18 V to the selected control gatate, respectively. The 18V applied to the selected cell's contrrol gates is coupled so that about 10 V is induced at the floatingg gate and 0.3 V is transferred to the selected cell's channelel. Then, a nearly 10 MeV field applied between the oppositte sides of a nearly 100 Å-thick tunnel oxide layer whiaich exists between the channel and floating gate, causes thhe floating gate electrode to be charged with electrons by thhe Fowler-Nordheim (F-N) tunnelling effect. Thus, a datum i is written into the selected memory cell.

Conversely, the erase operation, which is carricied out by discharging the electrons within the floating gate e electrode

to thereby lower the threshold voltage of the cell, is accomplished by applying 20 V to the P-well 2 on which the cell array is formed, opening the bit-line and source-line, and grounding the control gate. Thereby, the electrons within the floating gate are discharged by the field between the ends of the tunnel oxide layer. Here, in order to protect the transistor of the peripheral circuit which operates at +5 V (Vcc) from the approximately 20 V applied to the P-well 2 of the cell array during the erase operation, transistors are formed on another P-well 3 which is electrically isolated and independent of the P-well 2 of the cell array.

A read operation is performed according to the data determination. The data is determined by the bit-line current path fluctuating between "on" and "off" states according to the positive or negative value of the threshold voltage of the selected cells.

For manufacturing the above conventional NAND EEPROM device, a photolithography process for forming the well structures is performed twice: First, that is, for forming a first P-well 2 on which a cell array is to be formed and a second P-well 3 on which the NMOS transistor of the peripheral circuit is to be formed; Second for forming an N-well 4 which is located within the second P-well 3, on which the PMOS transistor of the peripheral circuit is to be formed on the N-type semiconductor substrate 1.

However, the conventional NAND EEPROM device as described above exhibits certain drawbacks. First, since the N-type substrate 1 is applied with a high voltage concurrently with the erase operation which applies 20 V to the P-well 2 on which the cell array exists, transistors cannot be formed directly on the N-type substrate 1. Also, since the transistors of the peripheral circuit are formed on a P-well 3 and an N-well 4 within this P-well 3, the bulk resistance is increased. Accordingly, latchup and other delitorious electrical characteristics occur.

SUMMARY OF THE INVENTION

For solving the above-mentioned problems, an object of the present invention is to provide a non-volatile memory device which can be manufactured by independently controlling the bulk regions used in the cell array and peripheral circuit regions thereof.

Another object of the present invention is to provide a suitable method for manufacturing a non-volatile memory device.

To accomplish the aforementioned objects, the present invention provides a semiconductor memory device comprising: a semiconductor substrate of a first conductivity type which is divided into a cell array region and a peripheral circuit region; a first impurity-doped region of the first conductivity type formed in the surface portion of the semiconductor substrate in the cell array region; a second impurity-doped region of a second conductivity type formed in the surface portion of the semiconductor substrate in the cell array region, the second impurity-doped region enclosing the first impurity-doped region; and a memory cell comprised of a fourth source region and a fourth drain region formed on the surface portion of the first impurity-doped region and of a floating electrode formed on the first impurity-doped region and a control electrode formed on the floating electrode. In the peripheral circuit region, the semiconductor memory device may further comprise a third impurity-doped region of the first conductivity type formed in a first surface portion of the semiconductor substrate in the peripheral circuit region; a first MOS transistor com-

prised of a first gate electrode formed on the thirird impurity-doped region and first source and drain regionsis formed in surface portions of the third impurity-doped regiciion; a second MOS transistor comprised of second source e and drain regions formed in a second surface portion of tthe semiconductor substrate in the peripheral circuit region aand a second gate electrode formed on the semiconductor s substrate; a fourth impurity-doped region of the second cconductivity type formed in a third surface portion of the semmiconductor substrate in the peripheral circuit region; a t third MOS transistor comprised of third source and drarain regions formed in surface portions of the fourth impurity-doped region and a third gate electrode formed on a the fourth impurity-doped region.

In order to achieve another object, the presennt invention provides a method for manufacturing a semmiconductor memory device comprising the steps of: provididing a semiconductor substrate of a first conductivity type d defined into a cell array region and a peripheral circuit regiciion; forming a second impurity-doped region of a second cconductivity type in a surface portion of the semiconductor s substrate in the cell array region; forming a first impurity-ddoped region of the first conductivity type enclosed by the firsrst impurity-doped region; and forming a memory device c on the first impurity-doped region. The memory device is s formed by forming a first conductive layer pattern on the firsrst impurity-doped region, forming an insulating layer patteern covering the first conductive layer pattern, forming a secoond conductive layer pattern on the insulating pattern, patatterning the second conductive layer pattern, the insulating lalayer pattern and the first conductive layer pattern sequentiallyly, to thereby form a control gate electrode and a floating gatete electrode, and implanting an impurity into the first impurity-doped region to thereby form a source region and a draiain region of the memory device.

In accordance with one embodiment of the preresent invention, in the peripheral circuit region, a third impurity-doped region of the first conductivity type in a first surfrface portion of the semiconductor substrate in the periphheral circuit region may be formed, and a fourth impurity-ddoped region of the second conductivity type in a third surfacece portion of the semiconductor substrate in the peripheral circrcuit may be formed.

The second and fourth impurity-doped regiorns are preferably formed by forming a first oxide layer orn the semiconductor substrate, forming an antioxidative llayer on the first oxide layer, forming a photoresist pattern c on the anti-oxidative layer which exposes portions of the antnti-oxidative layer where the second and fourth impurity-dopped regions are to be formed etching the exposed portions s of the anti-oxidative layer, and implanting a second conduuctivity type impurity into surface portions of the semiconductor substrate via the etched portion of the anti-oxidativive layer.

The first and third impurity-doped regions mayay be formed by forming a first oxide layer and an anti-oxidatitive layer on the semiconductor substrate excluding a portiorn where the second impurity-doped region is formed, formiring a second oxide layer on the second impurity-doped regiorn, forming a photoresist pattern exposing a portion of the seecond oxide layer where the first impurity-doped region is toto be formed and a portion of the anti-oxidative layer wherere the third impurity-doped region is to be formed, and then n implanting a first conductivity type impurity into the semmiconductor substrate.

According to one embodiment of the presentnt invention, the first conductivity type impurity is firstly impplanted at a first acceleration energy such that the first conductivity type impurity penetrates the second oxide layer and the anti-oxidative layer, and secondly implanted at a second acceleration energy such that the first conductivity type impurity penetrates the anti-oxidative layer but not the second oxide layer.

According to another embodiment of the present invention, the second oxide layer is etched using the photoresist pattern as an etching mask to thereby expose a surface portion of the semiconductor substrate where the first impurity-doped region is to be formed. The first conductivity type impurity is firstly implanted at a first acceleration energy such that the first conductivity type impurity does not penetrate the anti-oxidative layer, and secondly implanted at a second acceleration energy such that the first conductivity type impurity penetrates the anti-oxidative layer.

According to still another embodiment of the present invention, the first conductivity type impurity is firstly implanted at a first acceleration energy such that the first conductivity type impurity penetrates the anti-oxidative layer but not the second oxide layer, the second oxide layer is etched using the photoresist pattern as an etching mask to thereby expose a surface portion of the semiconductor substrate where the first impurity-doped region is to be formed, and then the first conductivity type impurity is secondly implanted at a second acceleration energy such that the first conductivity type impurity penetrates the anti-oxidative layer.

The NAND-structured EEPROM according to the present invention comprises EEPROM cells formed on the pocket P-well. The impurity concentration of the pocket P-well may be controlled independently from the P-well which is formed in the peripheral circuit region. Therefore, an EEPROM device having two P-wells in the cell array region and the peripheral circuit region, respectively, of which the concentrations may controlled according to the device characteristic and independently from each other, may be obtained.

Also, an NMOS transistor of the peripheral circuit region which is operated at a high voltage may be formed directly on the P-type semiconductor substrate, thus enhancing the resistance thereof against the high voltage. In the meantime, the characteristics of the NMOS transistor of the peripheral circuit region which is operated at Vcc, are controlled by forming the NMOS transistor on the P-well of the peripheral circuit region to thereby enhance the punch-through characteristics thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object and other advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a sectional view showing the conventional NAND-structured EEPROM;

FIG. 2 shows a portion of an equivalent circuit diagram of an EEPROM device using a conventional NAND-structured EEPROM cell and an erase and write (or program) operation thereof.

FIG. 3 is a sectional view showing a structure of a NAND-structured EEPROM according to one embodiment of the present invention;

FIGS. 4 through 12 are sectional views illustrating a method for manufacturing a NAND-structured EEPROM

device according to a first embodiment of thhe present invention;

FIGS. 13 and 14 are sectional views illustrating g a method for manufacturing a NAND-structured EEPRODM device according to a second embodiment of the present i invention;

FIG. 15 is a sectional view illustrating a mmethod for manufacturing a NAND-structured EEPROMM device according to a third embodiment of the present irinvention;

FIGS. 16 and 17 are sectional views illustrating g a method for manufacturing a NAND-structured EEPRODM device according to a fourth embodiment of the present i invention; and

FIG. 18 is a sectional view illustrating a mmethod for manufacturing a NAND-structured EEPROMM device according to a fifth embodiment of the present inmvention.

DESCRIPTION OF THE PREFERREDD EMBODIMENT

Hereinafter, the present invention is to be desscribed in more detail in reference with the attached drawinngs.

FIG. 3 is a sectional view of a NAND-s-structured EEPROM device according to one embodimeent of the present invention.

Into a semiconductor substrate of a first conductctivity type (having a low concentration), e.g., P-type semiiconductor substrate 10, a second conductivity type impurity ((an ion) is implanted to thereby form a plurality of second conductivity type impurity-doped regions, i.e., N-wells. Thesse N-wells include a first N-well 11 as a second impurity-dopped region (of a second conductivity type) formed in the (cell array region and a second N-well 12 as a fourth impurrity-doped region (of a second conductivity type) in a thirird surface portion of the semiconductor substrate in the ; peripheral circuit region.

A first conductivity type impurity is implanted i into a first N-well 11 of the cell array region, to thereby foiorm a first P-well 13 as a first impurity-doped region of a firsrst conductivity type in the cell array region. On first P-wvell 13, an EEPROM device having source and drain regionsns (formed in the surface portions of first P-well 13) and a flooating gate formed on the first P-well 13 and a control gate fiformed on the floating electrode, is formed. Since first NN-well 11 encloses first P-well 13, the first P-well 13 is ; generally referred to as a pocket P-well.

In the peripheral circuit region (having no cell aand including second N-well 12) of P-type semiconductor subbstrate 10, for operating the cell array, a second P-well 14 ; as a third impurity-doped region of a first conductivity type s is formed in a first surface portion of semiconductor substrtrate 10 by implanting an impurity having a first conductivity y type (the same conductivity type as that of semiconductor r substrate 10) into a first portion of the peripheral circuit t region of semiconductor substrate 10, while excluding thhe portion where second N-well 12 is formed.

On second P-well 14, a first MOS transistor (thhat is, first NMOS transistor) is formed which comprises fiirst source and drain regions formed in surface portions o of second P-well 14, and a first gate electrode formed on secoond P-well 14.

In a second portion of the peripheral circuit : region of P-type semiconductor substrate 10 (excluding thee portions where second N-well 12 and second P-well 14 arere formed), a second MOS transistor (second NMOS transiststor) which has a resistance against high voltage is formed between second P-well 14 and second N-well 12. The second MOS transistor includes second source and drain regions formed in second surface portions of semiconductor substrate 10 and a second gate electrode formed on semiconductor substrate 10.

On second N-well 12, a third MOS transistor (PMOS transistor) having third source and drain regions in surface portions of second N-well 12 and a third gate electrode on second N-well 12, are formed.

Since the second NMOS transistor is formed directly on the P-type semiconductor substrate 10, the reverse bias characteristic between the N+ doped region of the NMOS transistor and the P-type semiconductor substrate 10 having a low impurity concentration is improved. The second NMOS transistor has a gate insulating layer whose thickness is thicker than that of first NMOS transistor. Also, using a P-type semiconductor substrate 10 having a low impurity concentration improves the body effect. An NMOS transistor of the peripheral circuit, which does not have a resistance essentially against a high voltage, is formed on second P-well 14, thus improving the punch-through characteristic of the short channel.

The characteristic of second N-well 12 on which a PMOS transistor of the peripheral circuit is formed should be controlled according to the PMOS characteristic and the isolation characteristics thereof. Since second N-well 12 is formed simultaneously with the first N-well 11 wherein first P-well 13 (the pocket P-well) is to be formed, the change in the characteristics of second N-well 12 should accompany the characteristic change in first N-well 11. This in turn causes the characteristic of first P-well 13 to change. When simultaneously forming first P-well 13 and second P-well 14 by using the same photomask and the same ion-implantation processes, in order to optimize first P-well 13 according to the change in the characteristic of first N-well 11, the characteristic of second P-well 14 is undesirably changed. To solve this problem, a photolithography process should be added for forming first P-well 13 and second P-well 14 separately, which is undesirable.

In the present invention, a method for manufacturing the above EEPROM device without an additional photolithography process is provided. Hereinafter, the method will be described in detail with reference to the following embodiments.

Embodiment 1

FIGS. 4 through 12 are sectional views illustrating a method for manufacturing a NAND-structured EEPROM device according to a first embodiment of the present invention.

FIG. 4 is a sectional view illustrating a step of forming a first N-well 24 as a second impurity-doped region and a second N-well 24A as a fourth impurity-doped region in an upper surface portion of P-type semiconductor substrate 20. More particularly, on a first conductivity type semiconductor substrate, for example, <100>-oriented P-type semiconductor substrate 20 having a resistance of 18Ω.cm, a first oxide layer 21 is firstly formed to a thickness of 380 Å, as in the conventional N-well formation. Thereafter, on first oxide layer 21, a silicon nitride layer 22 as an anti-oxidative layer is formed by depositing silicon nitride to a thickness of about 2000 Å via a conventional chemical vapor deposition (CVD) method. Thereafter, a photoresist is coated on the silicon nitride layer 22 to thereby form a photoresist film (not shown). Then, the photoresist film is exposed using a

photomask for forming first and second N-well 2 24 and 24A and developed to form a first photoresist pattern (: (not shown) which exposes a portion of silicon nitride layer 222. Using the first photoresist pattern as an etching mask, a predetermined portion of silicon nitride layer 22 is etched, , to thereby expose surface portions of semiconductor ssubstrate 20 where first N-well 24 of the cell array region ı and second N-well 24A of the peripheral circuit region are to o be formed. Then, a second conductivity type impurity (N-typpe impurity) such as phosphor (P) is ion-implanted at a ı dosage of 1.7×10^{13} atoms/cm^2 and at an acceleration voltltage of 150 KeV, and then the first photoresist pattern is remmoved. Next, the substrate is heat-treated at a temperature of a about 1150° C. for seventeen hours, to thereby not only a activate the doped N-type impurity, but also diffuse the dopeed impurity into semiconductor substrate 20. As a result, firstst N-well 24 of the cell array region and second N-well 2 24A of the peripheral circuit region are formed.

Here, during the heat-treatment, second oxiddde layers 23 and 23A of the respective cell array region andd peripheral circuit region are grown to a thickness of 4,500 ÅÅ where the portions of silicon nitride layer 22 have been etetched.

FIG. 5 is a sectional view for illustrating a step p of forming a second photoresist pattern 26 for forming a firsrst P-well as a first impurity-doped region and a second P-welell as a third impurity-doped region, and then firstly implannting a first conductivity type impurity. After the step of FIG. ı. 4, a second photoresist is coated on the resultant, thereby y forming a second photoresist film. The second photoresesist film is exposed using a photomask for forming the first t and second P-wells and then developed to thereby formn a second photoresist pattern for forming the first and seccond P-wells which expose a portion (excluding the edge] portion) of second oxide layer 23 of the cell array region annd a portion of silicon nitride layer 22 where second P-wevell is to be formed. Then, a portion (excluding the surrounnding edge portions) of second oxide layer 23 of the cell aarray region which is formed on first N-well 24 is wet-etcheed using an oxide etchant, to thereby expose the surface ; portion of semiconductor substrate 20 where first N-well 2 24 has been formed. At this time, since silicon nitride layer 222 has a low etching selectivity with respect to the oxide etchhant used in the above wet-etching when compared to the seecond oxide layer 23, the exposed portion of silicon nitride layyer 25 is not etched away. Thereafter, a first conductivity type e impurity (a P-type impurity such as boron) is firstly ion-impplanted at a dosage of 0.9×10^{13} atoms/cm^2 and at a low a acceleration voltage of 50 KeV for forming the pocket P-welell of the cell array region. Under the above conditions, tthe exposed portion of silicon nitride layer 22 prevents the impurity from doping into the substrate. Thus, only a portion of f first N-well 24 is doped with P-type impurities via the exposed surface portion of semiconductor substrate 20.

FIG. 6 is a sectional view illustrating a step o of secondly implanting a first conductivity type impurity to thhereby form a first P-well 27 and a second P-well 27A. AAfter firstly implanting the first conductivity type impurityty at a low energy, in order to form second P-well 27A of thee peripheral circuit region, the same impurity as that firstly iimplanted is implanted at a dose of 1.5×10^{13} atoms/cm^2 at an a acceleration voltage of 130 KeV (by which boron can penetrtrate silicon nitride layer 22 having a thickness of about t 2,000 Å), without removing second photoresist pattern n 26. After removing second photoresist pattern 26, a driveve-in step is performed at a temperature of 1,150° C. for eight hours, to complete first (pocket) P-well 27 (as a first impurity-doped region) of the cell array area and second P-welell 27A (as a third impurity-doped region) of the peripheral circuit region. Second P-well 27A is formed in a first surface portion of semiconductor substrate 20 in the peripheral circuit region.

FIG. 7 is a sectional view illustrating a step of forming a plurality of field oxide layers 28, a first gate oxide layer 29 of the peripheral circuit region, a tunnel oxide layer 30 of the cell array region, and first polysilicon layer pattern 31 for forming floating electrode of a NAND-structured EEPROM cell of the cell array. More particularly, after the drive-in step of FIG. 6, silicon nitride layer 22, the 20 remaining second oxide layers 23 and 23A, and first oxide layer 21 are removed. Then, via a conventional LOCOS process, a plurality of field oxide layer 28 for electrically isolating devices are formed on semiconductor substrate 20, and then a first gate oxide layer 29 is formed to a thickness of 200 Å on the whole surface portion of semiconductor substrate 20 excluding the portions where field oxide layers 28 have been formed. Next, in order to selectively form tunnel oxide layer 30 in the cell array region which is thinner than first gate oxide layer 29, a portion of first gate oxide layer 29 in the cell array region is removed via a conventional photolithography process. After removing the photoresist pattern used in the photolithography process, a tunnel oxide layer 30 is formed to a thickness of 100 Å on first P-well of cell array region. Thereafter, for forming a first conductive layer for forming a floating gate of an EEPROM device, a first polysilicon is deposited to a thickness of 1,500 Å, to thereby form a first polysilicon layer. The first polysilicon layer is doped with phosphorous ions so as to have a sheet resistance of 100Ω/□, thereby forming a first conductive layer for forming the floating gate. Then, the first conductive layer is patterned by a conventional photolithography process, to thereby form a first conductive layer pattern 31 on the cell array region.

FIG. 8 is a sectional view illustrating an insulating layer pattern 32 covering first conductive layer pattern 31 and implanting an impurity for controlling the threshold voltage of the peripheral circuit region. After the step of FIG. 7, an oxide/nitride/oxide (ONO) layer is formed to a thickness of 160 Å/200 Å/30 Å as an insulating layer on the whole surface of the resultant. Thereafter, a third photoresist pattern 33 is formed which covers the cell array region and exposes the peripheral circuit region. Using third photoresist pattern as an etching mask, the ONO film is etched to thereby form insulating layer pattern 32 covering first conductive layer pattern 31. At this time, first gate oxide layer 29 which is formed on the peripheral circuit region, is simultaneously removed, to thereby expose the surface of semiconductor substrate 20 of the peripheral circuit region.

Thereafter, in order to control the threshold voltage of peripheral circuit region, while leaving third photoresist pattern 33, a first conductivity type (P-type) impurity, such as boron, is ion-implanted through the exposed surface of semi-conductor substrate 20 at a dosage of 2.0×10^{11} atoms/cm^2 and at an acceleration voltage of 50 KeV, and then third photoresist pattern 33 is removed.

Thereafter, an ion-implantation process is performed for differentiating the threshold of the NMOS transistors of the peripheral circuit. More particularly, a region where an NMOS transistor of the peripheral circuit is to be formed, i.e., second P-well 27A, is exposed by forming a fourth photoresist pattern (not shown) and then, a first conductivity type (P-type) impurity, such as boron, is ion-implanted through the exposed region at a dosage of 6.0×10^{11} atoms/cm^2 and at an acceleration voltage of 50 KeV. Thereafter, the fourth photoresist pattern is removed.

Then, in order to form a normally on (operable) NMOS transistor of the peripheral circuit directly on semiconductor

substrate **20** (but not on second N-well **24A** nnor second P-well **27A**), a fifth photoresist pattern (not s shown) is formed to expose a portion of semiconductor subbstrate **20** between second P-well **27A** and second N-well 2224A in the peripheral circuit section. Through the exposed portion, a second conductivity type (N-type) impurity such a as arsenic (As) is ion-implanted at a dosage of 2.2×10^{12} atomns/cm^2 and at an acceleration voltage of 30 KeV. Next, the fififth photoresist pattern is removed.

FIG. **9** is a sectional view illustrating a step of f forming a second gate oxide layer **34** and partially removining second gate oxide layer **34** on second N-well **24A** and secoond P-well **27A**. After removing the fifth photoresist patterrn, second gate oxide layer **34** is grown to a thickness of 2000 Å via a thermal oxidation, on the whole surface of the e resultant excluding the cell array region where insulating layyer pattern **32** covers. Thereafter, a photoresist is coated on thee resultant to form a photoresist film, which is exposed usingg a photomask and then developed to form a sixth photoresisist pattern **35** exposing a portion of second gate oxide layer **334** formed on both second N-well **24A** and second P-well **277A**. Using sixth photoresist pattern **35** as an etching mask, thee exposed portion (which is formed in the peripheral circuit region excluding the region where a PMOS transistoor and an NMOS transistor having a resistance against a hig gh voltage are to be formed) of second gate oxide layer **34** o on second P-well **27A** and second N-well **24A**, is partially remmoved via a conventional etching method.

FIG. **10** is a sectional view illustrating a step obf forming a third gate oxide layer **36** and forming gate electrrodes **39***a*, **39***b* and **39***c* of the transistors of the peripheral circcuit and a composite conductive pattern **39***b* for forming coontrol gate electrodes of the cell array EEPROMs. After removving sixth photoresist pattern **35**, on the surface region o of second P-well **27A** and second N-well **24A** (where seccond gate oxide layer **34** has been etched), third gate oxide llayer **36** is grown to have a thickness of about 180 Å, via a conventional thermal oxidation process. During the thermal oxicidation for forming third gate oxide layer **36**, second gate oxidde layer **34** (which is formed between second P-well **27A** annd second N-well **24A** and has not **5** been etched in the abovve step of FIG. **9**) grows to a greater thickness than itsts original thickness of 200 Å. Reference numeral **34'** repreresents the additionally grown second gate oxide layer.

Thereafter, on whole surface of the resultant, as is a second conductive layer for forming the control gate elecctrodes of the cell array and the gate electrodes of the transisistor of the peripheral circuit, a second polysilicon is depositeed to form a second polysilicon layer having a thickness of abbout 1,500 Å, and then phosphorous is doped so that thhe second polysilicon layer has a sheet resistance of 100Ω/□.]. Then, on the second polysilicon layer, a refractory metal silidicide layer is formed by depositing a refractory metal silicidele (such as WSi) to a thickness of 1,500 Å. Thereafter, the c composite conductive layer consisting of the second polysilidicon layer and the refractory metal silicide layer is patternmed via a photolithography process using a seventh photoresisist pattern **40**. Thus, first, second and third gate electrodes **39***da*, **39***b* and **39***c* of first, second and third MOS transistors of thhe peripheral circuit consisting of first, second and third patttterns **37***a*, **37***b* and **37***c* of second polysilicon layer pattern ı and first, second and third refractory metal silicide layer patattern **38***a*, **38***b* and **38***c* are formed. Also, a composite patternn **39***d* for forming control gate electrode of the cell arraay (which covers insulating layer pattern **32**) consisting of f a fourth second polysilicon layer pattern **37***d* and fourth r refractory metal silicide layer pattern **38***d*, is formed.

According to the above method, since the NMOS transistor's gate formed directly on P-type semiconductor substrate **20** which operates at a high voltage of about 20 V during the cell program/erase operation, has the thickly grown second gate oxide layer **34'** as a gate oxide layer, its resistance against high voltage is improved. In the meantime, the NMOS transistor formed on second P-well **27A** which operates at Vcc (which is a low voltage) uses third gate oxide layer **36** as a gate insulating layer (which is relatively thin when compared to that of the NMOS transistor formed directly on semiconductor substrate **20**). Therefore, the punch-through characteristic the NMOS transistor is improved.

FIG. **11** is a sectional view illustrating a step of forming a control gate electrode **42** and a floating gate electrode **31A** of the cell array. After removing sixth photoresist pattern **40** in FIG. **10**, a seventh photoresist pattern **43** for forming the control and floating electrode of an EEPROM which covers the peripheral circuit region is formed on the resultant. Using seventh photoresist pattern **43** as an etching mask, fourth refractory metal silicide layer pattern **38***d*, second polysilicon layer pattern **37***d*, insulating layer pattern **32** and first polysilicon layer pattern **31** are sequentially etched to thereby form the floating gate electrode **31A** and control gate electrode **42** (consisting of a fifth second polysilicon layer pattern **37***e* and a fifth refractory metal silicide layer pattern **38***e*) of the cell array.

FIG. **12** is a sectional view illustrating a step of completing the EEPROM cells and first, second and third MOS transistors of the peripheral circuit. After removing seventh photoresist pattern **43**, N-type and P-type impurities are ion-implanted to the resultant, and heat-treatment is performed for activating and diffusing the implanted ions via a conventional MOS transistor-forming process. Therefore, an EEPROM cell consisting of floating gate electrode **31A** formed on first P-well **27**, a control gate electrode **42** formed on floating gate electrode **31A**, and a fourth source and drain regions **44***d* is formed. In the peripheral circuit region, a first MOS transistor (an first NMOS transistor) consisting of first gate electrode **39***a* formed on second P-well **27A**, and first source and drain regions formed in the surface portions of second P-well **27A** is formed. Also, on a second portion of semiconductor substrate **20** in the peripheral circuit region, a second MOS transistor (a second NMOS transistor) consisting of second gate electrode **39***b* and second source and drain regions **44***a* formed in the second surface portions of semiconductor substrate **20** in the peripheral circuit region, is formed. On second 15N-well **24A**, a third MOS transistor (a PMOS transistor of the peripheral circuit) consisting of a third gate electrode **39***c* formed on second N-well **24A** and a third source and drain regions **44***c* formed in the surface portions of second N-well, is formed. Thus, two NMOS transistors and one PMOS transistor of the peripheral circuit are formed in the peripheral circuit region.

Subsequent steps (not shown) such as a metallization process, a process for forming insulation interlayer, and a planarization process, are performed to thereby complete the EEPROM device of the present invention, in the same manner as in the case of a conventional memory device. Therefore, detailed descriptions thereof will be omitted.

Embodiment 2

FIGS. **13** and **14** are sectional views illustrating a method for manufacturing a NAND-structured EEPROM device according to a second embodiment of the present invention.

FIG. 13 is a sectional view illustrating a stetep of firstly implanting a first conductivity type impurity.

The same procedure as shown in FIG. 4 of EEmbodiment 1 is performed. After forming second photoresisist pattern 26 in the same manner as in Embodiment 1, bmoron is ion-implanted at a dosage of 1.5×10^{13} atoms/cm^2 and at an acceleration energy such that the boron penetrates first and second oxide layers 21 and 23 and silicon nitriride layer 22, for example, at an acceleration voltage of 240) KeV.

FIG. 14 is a sectional view illustrating a step p of secondly implanting a first conductivity type impurity. AAfter the step of FIG. 13, boron is ion-implanted at a dose of 0 0.5×10^{13} and at an acceleration energy such that the boromn penetrates silicon nitride layer 22 but not second oxide layeyer 23, i.e., at an acceleration voltage of 130 KeV. Thereafter, r, in the same manner as in Embodiment 1, after removing seecond photoresist pattern 26, a drive-in step is performmed, to thus complete first (pocket) P-well 27 of the cell arrray area and second P-well 27A of the peripheral circuit reggion.

Thereafter, subsequent steps are performed i in the same manner as described with respect to FIGS. 7 thhrough 12 of Embodiment 1, so the detailed descriptions thereeof omitted.

Embodiment 3

FIG. 15 is a sectional view illustrating a ı method for manufacturing a NAND-structured EEPRCOM device according to a third embodiment of the presentıt invention.

FIG. 15 is a sectional view illustrating a step p of implanting a first conductivity type impurity. In Embodiiments 1 and 2, the first conductivity type impurity is implannted via two implantation steps. However, in the present embooodiment, the first conductivity type impurity is implanted juust once.

After forming second photoresist pattern 26 annd removing the exposed second oxide layer 23 by the wet-etetching in the same manner as in Embodiment 1, for forming g first P-well 27 and second P-well 27A, boron is implanted i at a dose of 1.5×10^{13} atoms/cm^2 and at an acceleration energrgy such that the boron penetrates silicon nitride layer 22, for r example, at an acceleration voltage of 240 KeV. With chhanging the thickness of silicon nitride layer 22, the doped aramount of the impurity (that is, boron) which forms second l P-well 27A may be controlled.

Thereafter, the subsequent steps are performmed in the same manner as in Embodiment 1 (i.e., thosse shown in FIGS. 7 through 12).

Embodiment 4

FIGS. 16 and 17 are sectional views illustratiring a method for manufacturing a NAND-structured EEPRROM device according to a fourth embodiment of the presennt invention.

FIG. 16 is a sectional view illustrating a stetep of firstly implanting a first conductivity type impurity. Aftfter performing the step of FIG. 4 of Embodiment 1, seconnd photoresist pattern 26 is formed in the same manner as in EEmbodiment 1. Thereafter, boron is ion-implanted at a dosage e of 1.5×10^{13} atoms/cm^2 and at an acceleration energy such h that boron penetrates silicon nitride layer 22 but not seconnd oxide layer 23, for example, at an acceleration voltage of 2 240 KeV.

FIG. 17 is a sectional view illustrating a step o of secondly implanting a first conductivity type impurity. AAfter the step of FIG. 16, the exposed portion of second oxidele layer 23 is removed by the wet-etching, and then boronn is ion-implanted at a dosage of 1.0×10^{13} and at an acceleraration energy such that boron penetrates silicon nitride layayer 22, for example, at an acceleration energy of 240 KeV. Thereafter, a drive-in step is performed in the same manner as in Embodiment 1, to thereby form first P-well 27 and second P-well 27A.

The subsequent steps are performed in the same manner as those of FIGS. 7 through 12. Accordingly, the detailed descriptions thereof are omitted.

Embodiment 5

FIG. 18 is a sectional view illustrating~ a method for manufacturing a NAND-structured EEPROM device according to a fifth embodiment of the present invention.

In the present embodiment, controlling the concentration of the impurity for forming first P-well 27 and second P-well 27A separately and independently, is 5 unnecessary.

FIG. 18 is a sectional view illustrating a step of implanting a first conductivity type impurity. After performing the step of FIG. 4 of Embodiment 1, nitride layer 22 (which is used as an anti-oxidative layer) and first oxide layer 21 are removed by wet etching, thereby exposing the whole surface of semiconductor substrate 20. Thereafter, an oxide layer 23B is grown to a thickness of about 500 Å via a conventional thermal oxidation. Then, second photoresist pattern 26 is formed in the same manner as in Embodiment 1, to thereby expose the portions of oxide layer 23B where first P-well and second P-well are to be formed.

Next, boron is ion-implanted at a dosage of 1.5×10^{13} and at an acceleration energy such that boron penetrates oxide 23B.

The subsequent steps are performed in the same manner as those of FIGS. 7 through 12. Accordingly, the detailed descriptions thereof are omitted.

The NAND-structured EEPROM device according to the present invention comprises EEPROM cells formed on a pocket P-well. The impurity concentration of the pocket P-well is controlled independently form the P-well formed in the peripheral circuit region. Therefore, an EEPROM device having two P-wells in the cell array region and the peripheral circuit peripheral circuit region of which the concentrations may controlled according to device characteristics and independently from each other, can be obtained.

According to one embodiment of the present invention, an NMOS transistor of the peripheral circuit region which is operated at a high voltage is formed directly on the P-type semiconductor substrate. Therefore, the resistance thereof against the high voltage is enhanced. Further, an NMOS transistor of the peripheral circuit region which is operated at Vcc, is formed on the P-well of the peripheral circuit region the characteristics of which are controlled independently from the P10 well of the cell array region. This enhances the punch-through characteristic.

Also, according to a method for manufacturing a NAND structured EEPROM memory device, using only a twice-performed photolithography process may separately and independently control the characteristics of the P-wells of the cell array region and the peripheral circuit region. Therefore, the characteristics of the P-wells are differentiated so that the transistor characteristic of the peripheral circuits can be differentiated.

Consequently, the present invention can provide a non-volatile semiconductor memory device having an excellent characteristic in spite of the shortened steps of the whole process.

While the present invention has been particularly shown and described with reference to particular embodiments

thereof, it will be understood by those skilled in the art that various changes in form and details may be effected therein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. An EEPROM semiconductor memory device comprising:

a semiconductor substrate having a first conductivity type, said semiconductor substrate being divided into a cell array region and a peripheral circuit region;

a first impurity-doped region having said first conductivity type formed in a first surface portion of said semiconductor substrate in said cell array region;

a second impurity-doped region having a second conductivity type formed in said first surface portion of said semiconductor substrate in said cell array region, said second impurity-doped region enclosing said first impurity-doped region;

a memory cell comprising:

a memory source region and a memory drain region formed on a surface portion of said first impurity-doped region, and

a floating electrode formed on said first impurity-doped region and a control electrode formed on said floating electrode;

a third impurity-doped region having said first conductivity type formed in a first surface portion in said peripheral circuit region of said semiconductor substrate;

a first MOS transistor comprising:

first source and drain regions formed in respective surface portions of said third impurity-doped region, and

a first gate electrode formed on said third impurity-doped region; a second MOS transistor comprising:

second source and drain regions formed directly in respective second surface portions in said peripheral circuit region of said semiconductor substrate, and

a second gate electrode formed on said semiconductor substrate;

a fourth impurity-doped region having said second conductivity type and being formed in a third surface portion in said peripheral circuit region of said semiconductor substrate; and

a third MOS transistor comprising:

third source and drain regions formed in respective surface portions of said fourth impurity-doped region, and

a third gate electrode formed on said fourth impurity-doped region.

2. The EEPROM semiconductor memory device according to claim 1, wherein said first and second MOS transistors are NMOS transistors, and said third MOS transistor is a PMOS transistor.

3. The EEPROM semiconductor memory device according to claim 1, wherein a first gate insulating film of said second MOS transistor is thicker than a second gate insulating film of said first MOS transistor.

4. The EEPROM semiconductor memory device according to claim 1, wherein said second MOS transistor is formed between said first MOS transistor and said third MOS transistor.

5. The EEPROM semiconductor memory device according to claim 1, wherein a first impurity concentration of said first impurity-doped region is controlled independently from a second impurity concentration of said third impurity-doped region.

6. The EEPROM semiconductor memory device according to claim 1, wherein said first conductivity type is P-type and said second conductivity type is N-type.

7. An EEPROM semiconductor memory device comprising:

a P-type semiconductor substrate which is divided into a cell array region and a peripheral circuit region;

a first P-well formed in a surface portion in said cell array region of said semiconductor substrate;

a first N-well formed in said surface portion in said cell array region of said semiconductor substrate, said first N-well enclosing said first P-well;

a memory cell comprising:

a memory source region and a memory drain region formed on a surface portion of said first P-well,

a floating electrode formed on said first P-well, and

a control electrode formed over said floating electrode;

a second P-well formed in a first surface portion of said peripheral circuit region of said semiconductor substrate;

a first NMOS transistor comprising:

first source and drain regions formed in respective surface portions of said second P-well, and

a first gate electrode formed on said second P-well;

a second NMOS transistor comprising:

second source and drain regions formed directly in a second surface portion of said peripheral circuit region of said semiconductor substrate, and

a second gate electrode formed on said second surface portion of said peripheral circuit region of said semiconductor substrate;

a second N-well formed in a third surface portion of said peripheral circuit region of said semiconductor substrate; and

a PMOS transistor comprising:

third source and drain regions formed in a surface portion of said second N-well, and

a third gate electrode formed on said second N-well.

8. The EEPROM semiconductor memory device according to claim 7, wherein said first N-well and said second N-well are formed substantially simultaneously, and said first P-well and said second P-well are formed substantially independently.

9. The EEPROM semiconductor memory device according to claim 1, wherein said first impurity-doped region and said third impurity-doped region are formed substantially simultaneously, and said second impurity-doped region and said fourth impurity-doped region are formed substantially independently.

* * * * *

US005546341A

United States Patent [19]

Suh et al.

[11] Patent Number: 5,546,341

[45] Date of Patent: Aug. 13, 1996

[54] **NONVOLATILE SEMICONDUCTOR MEMORY**

[75] Inventors: **Kang D. Suh**, Ahnyang; **Jin K. Kim**, Seoul; **Jeong H. Choi**, Kwacheon, all of Rep. of Korea

[73] Assignee: **Samsung Electronics Co., Ltd.**, Suwon, Rep. of Korea

[21] Appl. No.: **441,477**

[22] Filed: **May 15, 1995**

Related U.S. Application Data

[62] Division of Ser. No. 171,300, Dec. 22, 1993, Pat. No. 5,473,563.

[30] **Foreign Application Priority Data**

Jan. 13, 1993 [KR] Rep. of Korea 390/1993

[51] **Int. Cl.**[6] **G11C 16/00**

[52] **U.S. Cl.** **365/185.33**; 365/185.29; 365/218

[58] **Field of Search** 365/185, 218, 365/900, 185.29, 185.33

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(List continued on next page.)

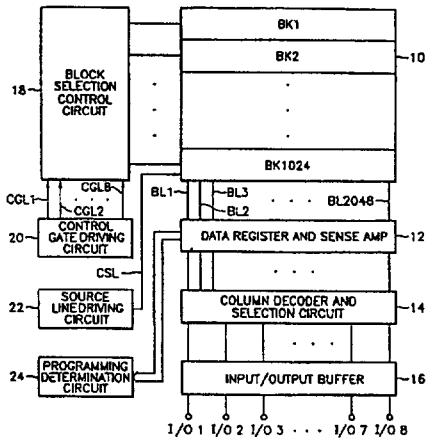
Primary Examiner—Tan T. Nguyen

Attorney, Agent, or Firm—Cushman, Darby & Cushman, L.L.P.

[57] **ABSTRACT**

A nonvolatile semiconductor memory device comprising an array of cell units, each cell unit including at least one memory transistor which has a floating gate and a control gate, the array being divided into a plurality of memory blocks each having a certain number of cell units. A selected memory block is erased by an erase voltage applied to a semiconductor substrate while unselected memory blocks are prevented from erasing by capacitive coupling of the erase voltage to floated word lines connected to control gates of memory transistors of the unselected memory blocks. In a program mode where a program voltage is applied to a selected word line of a selected memory block and a pass voltage is applied to unselected word lines of the selected memory block, channel regions and source and drain junctions of memory transistors of cell units in the selected memory block are charged to a program inhibition voltage. Channel regions and source and drain junctions of cell units associated with memory transistors programmed to the other binary data are discharged to be programmed while those of cell units associated with nonprogrammed memory transistors are maintained to the program inhibition voltage to prevent programming.

9 Claims, 18 Drawing Sheets



EXHIBIT

tabbies

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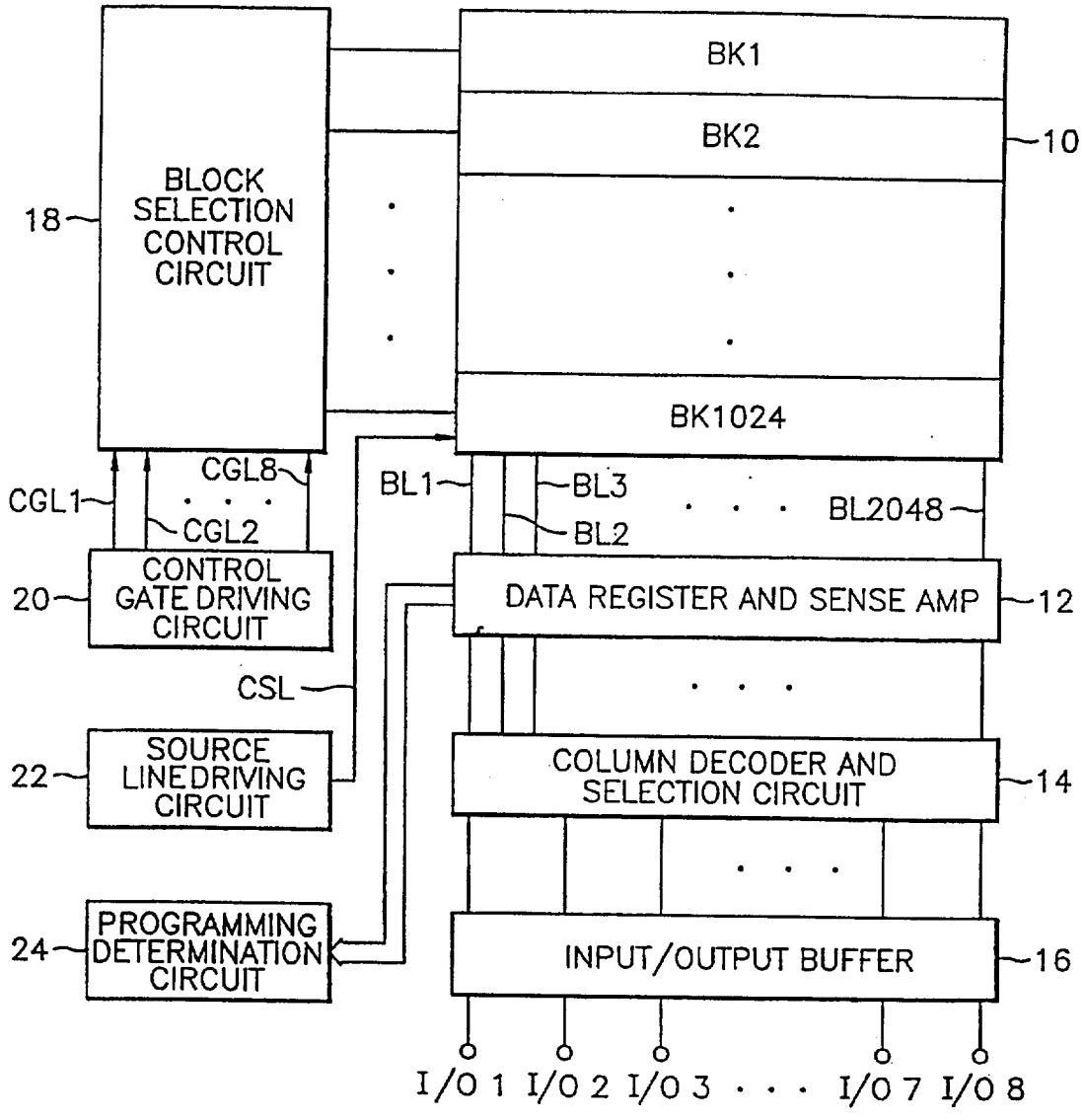
BK1
BK2
BK1024
10
BLOCK SELECTION CONTROL CIRCUIT
18
CGL1
CGL2
CGL8
BL1
BL2
BL3
BL2048
CONTROL GATE DRIVING CIRCUIT
20
DATA REGISTER AND SENSE AMP
12
CSL
SOURCE LINE DRIVING CIRCUIT
22
COLUMN DECODER AND SELECTION CIRCUIT
14
PROGRAMMING DETERMINATION CIRCUIT
24
INPUT/OUTPUT BUFFER
16
I/O 1 I/O 2 I/O 3 · · · I/O 7 I/O 8

FIG. 1

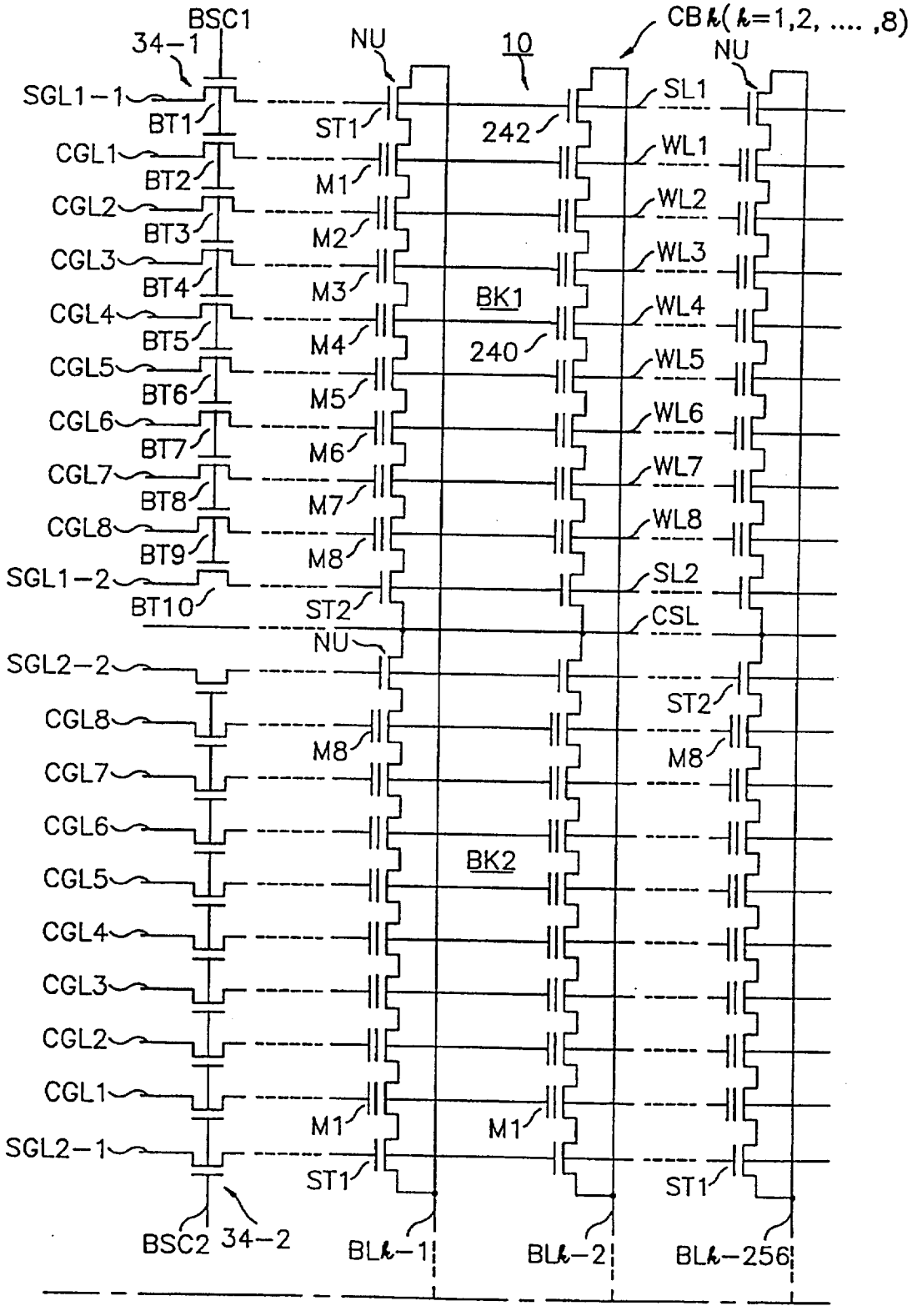
BSC1
34-1
NU
10
CBk(k=1,2, ... ,8)
NU
SGL1-1
BT1
ST1
242
SL1
CGL1
BT2
M1
WL1
CGL2
BT3
M2
WL2
CGL3
BT4
M3
BK1
WL3
CGL4
BT5
M4
240
WL4
CGL5
BT6
M5
WL5
CGL6
BT7
M6
WL6
CGL7
BT8
M7
WL7
CGL8
BT9
M8
WL8
SGL1-2
BT10
ST2
SL2
CSL
NU
SGL2-2
CGL8
M8
ST2
CGL7
M8
CGL6
CGL5
BK2
CGL4
CGL3
CGL2
CGL1
M1
M1
SGL2-1
ST1
ST1
BSC2
34-2
BLk-1
BLk-2
BLk-256

FIG. 2a

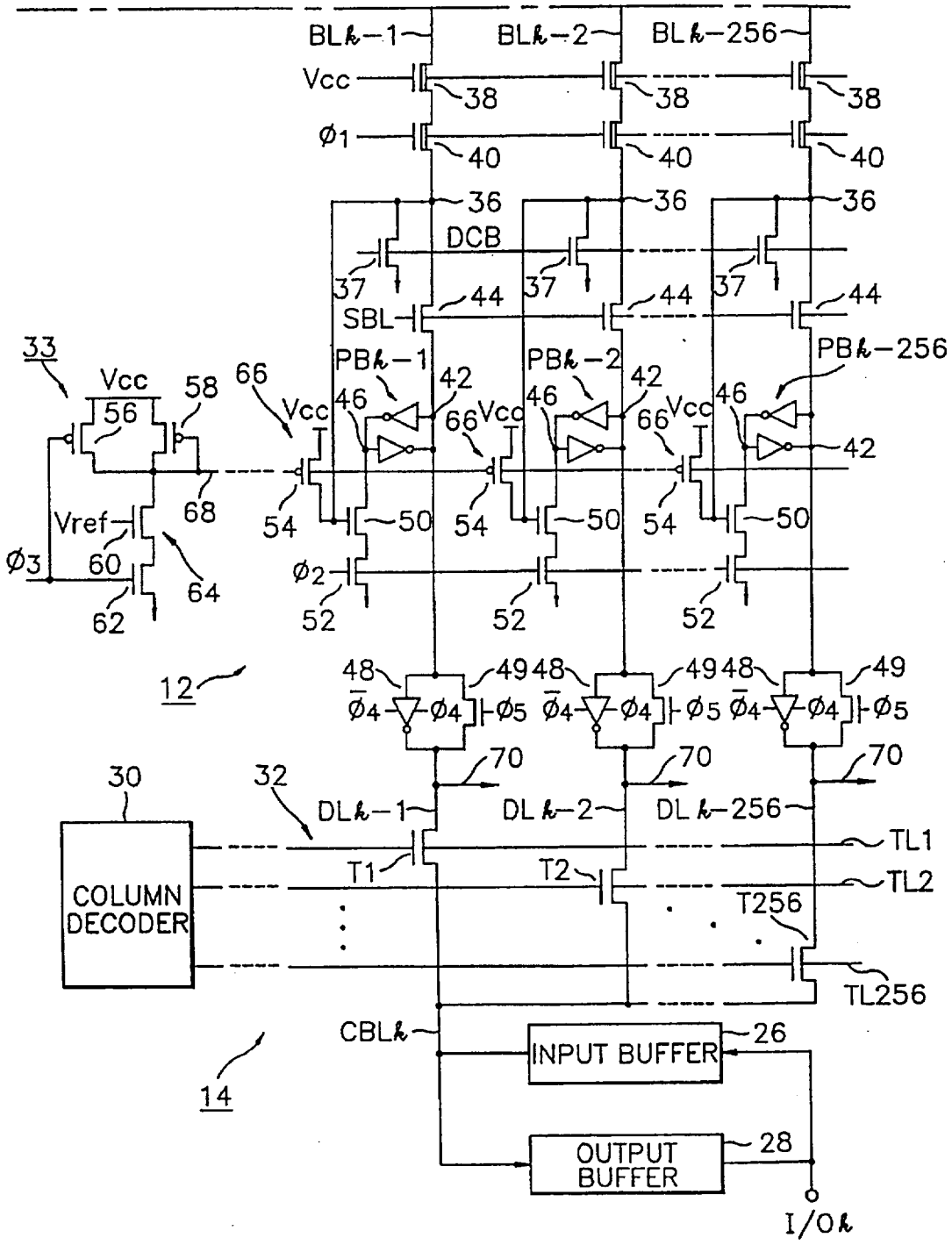
BLk−1
BLk−2
BLk−256
Vcc
38
Ø1
40
36
DCB
37
SBL
44
33
PBk−1
PBk−2
PBk−256
42
46
66
58
56
68
Vref
60
64
62
54
50
Ø2
52
Ø3
12
48
49
Ø4
Ø5
70
30
32
DLk−1
DLk−2
DLk−256
TL1
TL2
TL256
T1
T2
T256
COLUMN DECODER
CBLk
INPUT BUFFER
26
OUTPUT BUFFER
28
I/Ok
14

FIG. 2b

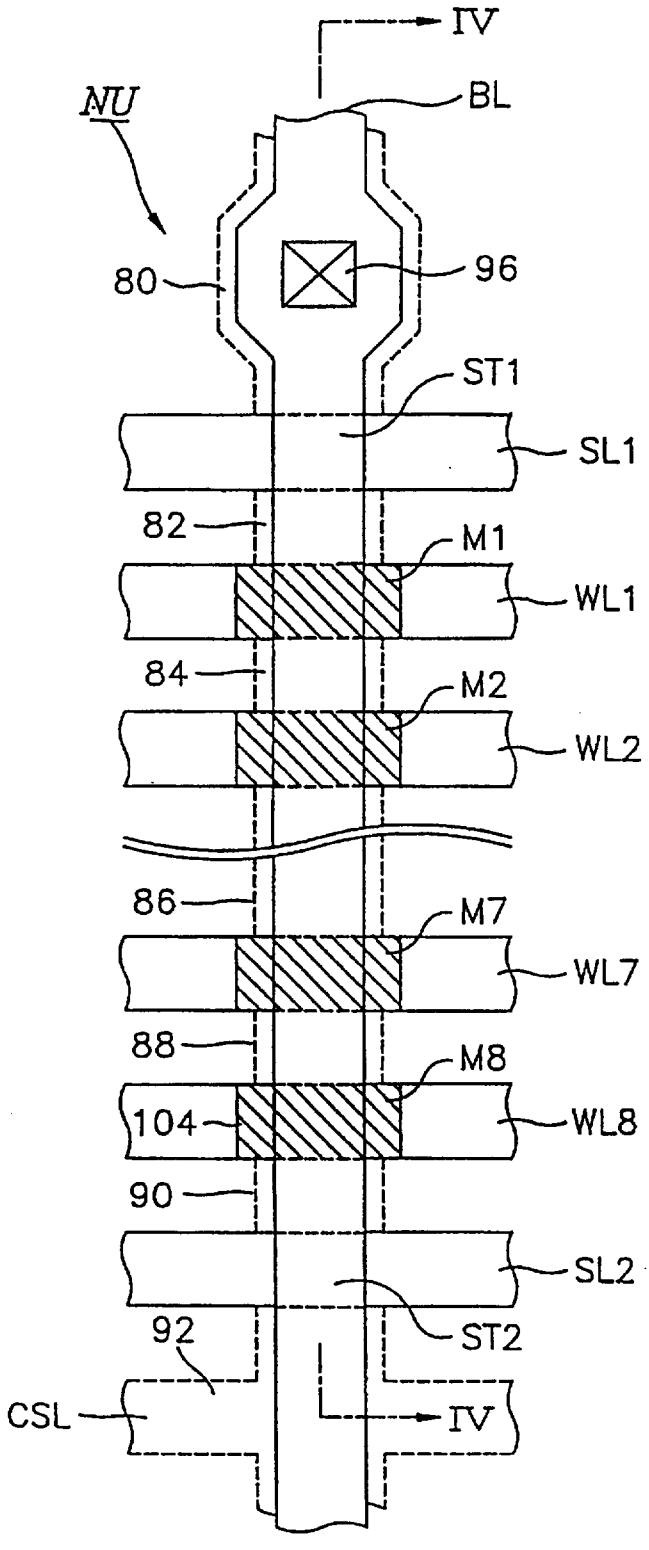
IV
NU
BL
80
96
ST1
SL1
82
M1
WL1
84
M2
WL2
86
M7
WL7
88
M8
104
WL8
90
SL2
92
ST2
CSL
IV

FIG. 3

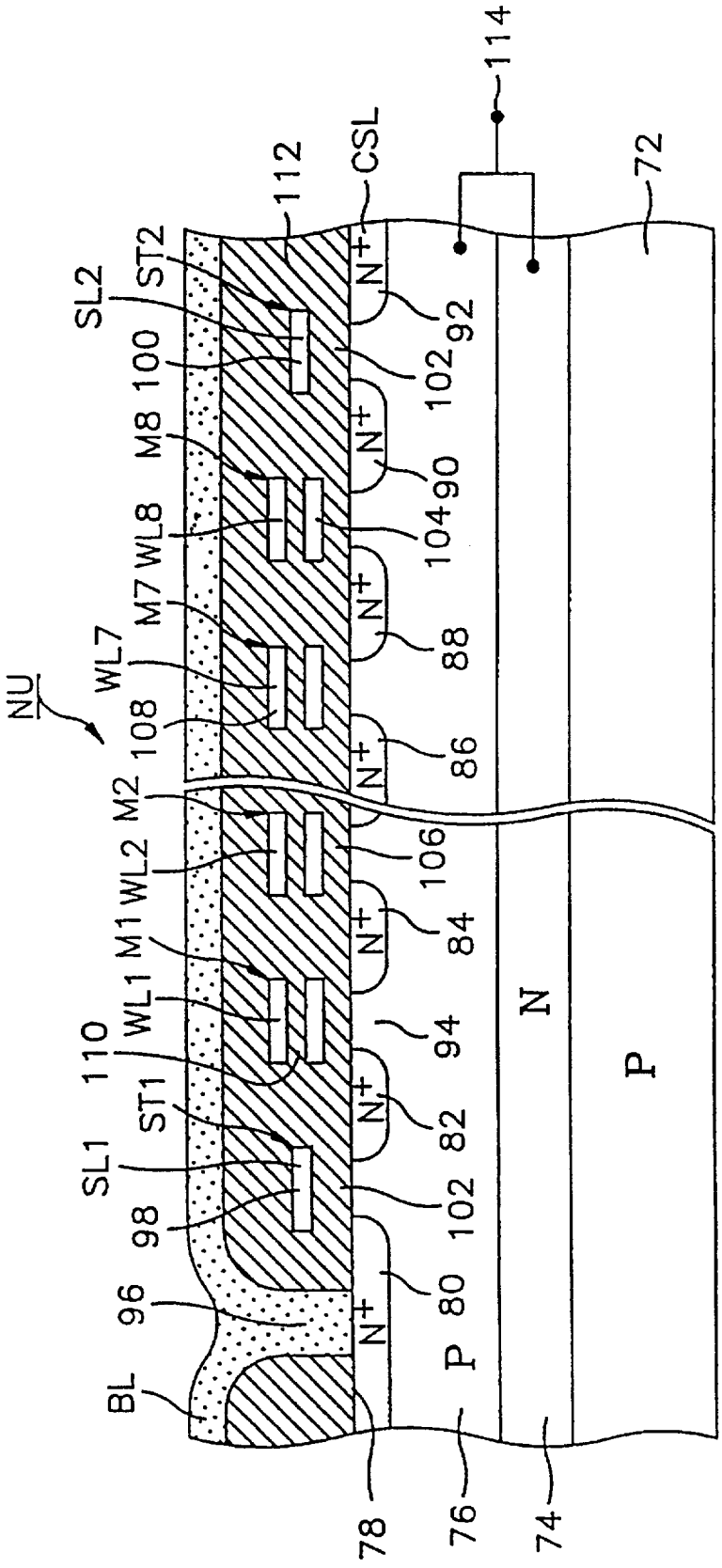
114
CSL
112
72
SL2
ST2
M8
WL8
M7
WL7
NU
M2
WL2
M1
WL1
SL1
ST1
110
BL
100
108
106
104
102
98
96
92
90
88
86
84
82
94
80
N+
P
N
P
78
76
74

FIG. 4

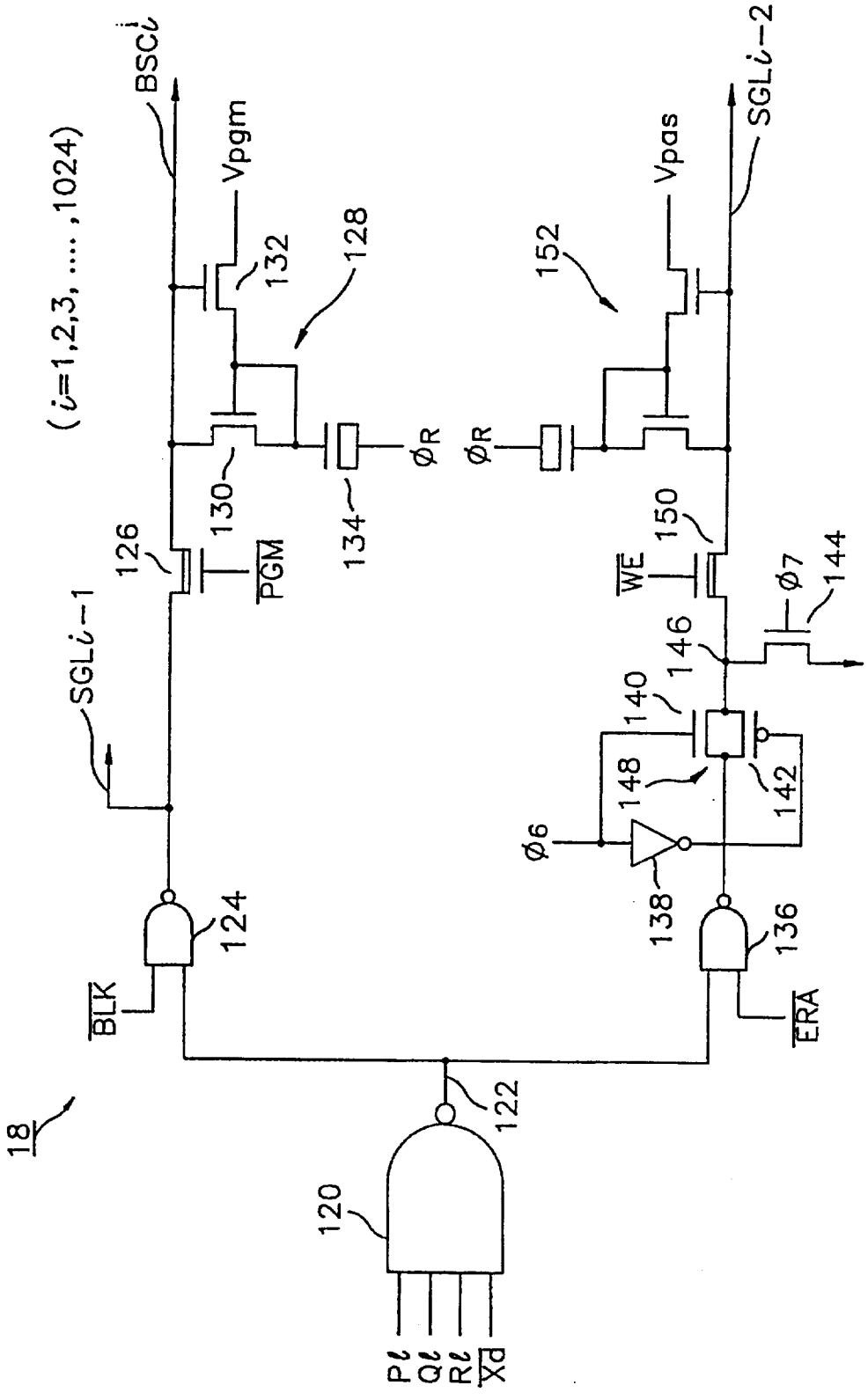
BSCi
(i=1,2,3, ... ,1024)
Vpgm
132
128
130
134
φR
126
PGM
SGLi-1
124
BLK
18
120
122
Pi
Qi
Ri
Xd
152
Vpas
SGLi-2
φR
150
WE
φ7
144
146
140
148
142
φ6
138
136
ERA

FIG. 5

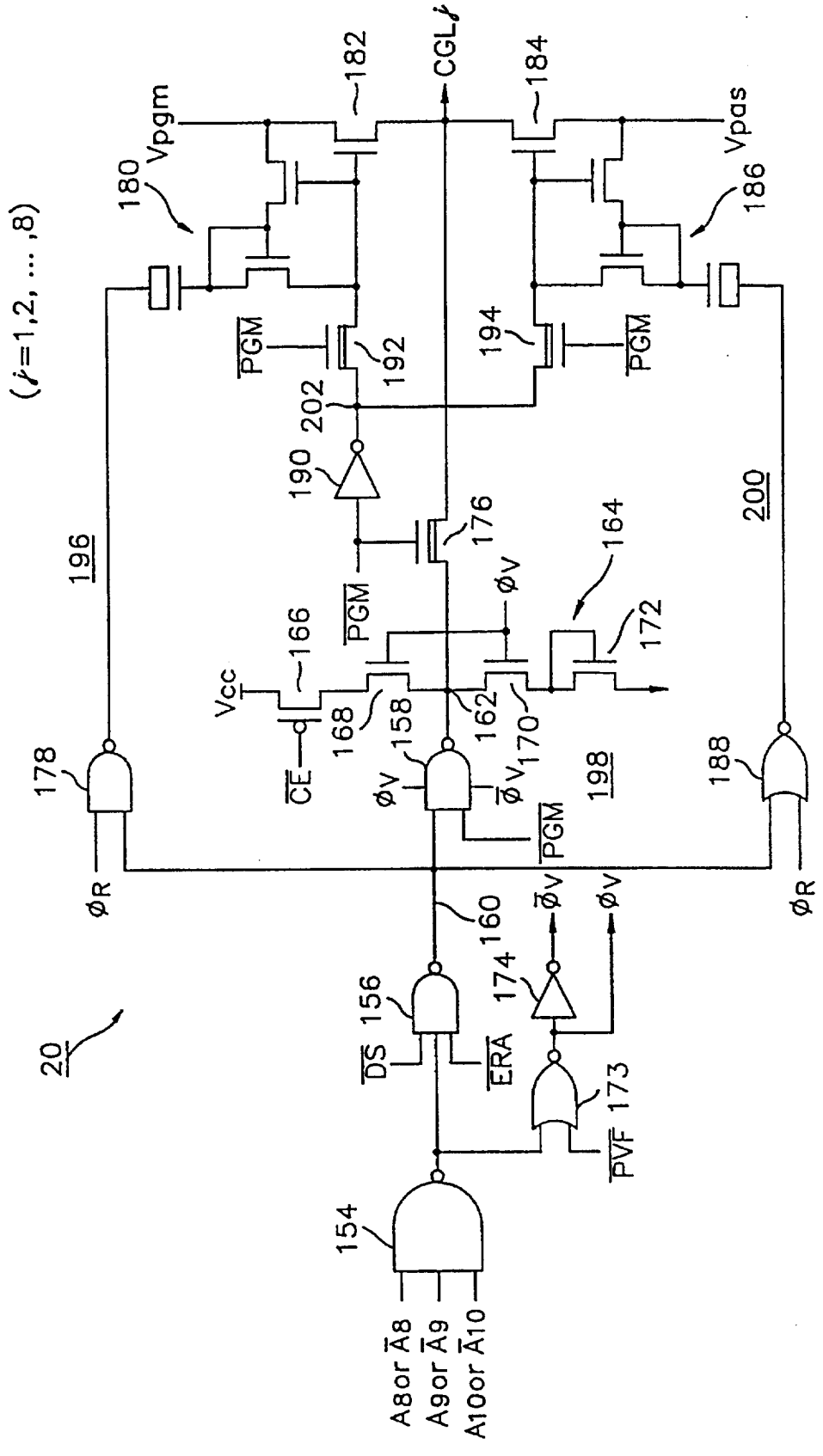
(i=1,2, ... ,8)
CGLi
182
184
Vpgm
Vpas
180
186
PGM
192
194
202
190
176
164
196
200
166
172
Vcc
168
158
162
170
178
188
CE
198
20
160
174
156
173
154
A8 or Ā8
A9 or Ā9
A10 or Ā10

FIG. 6

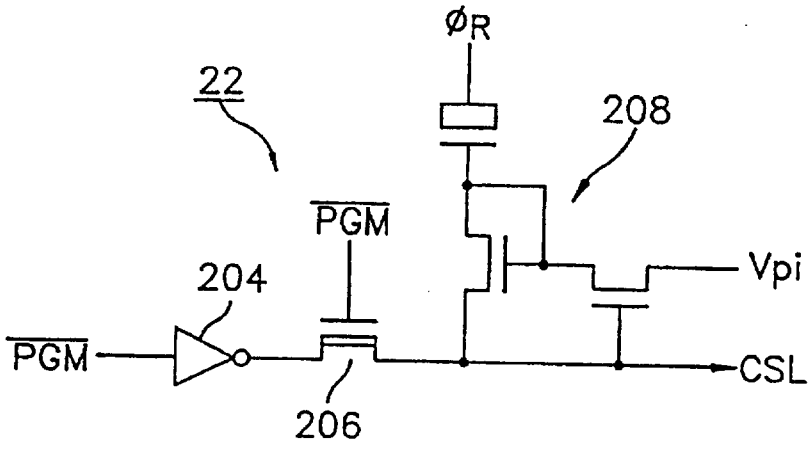

FIG. 7

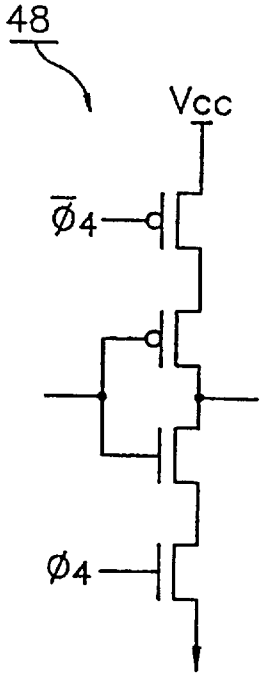

FIG. 8a

FIG. 8

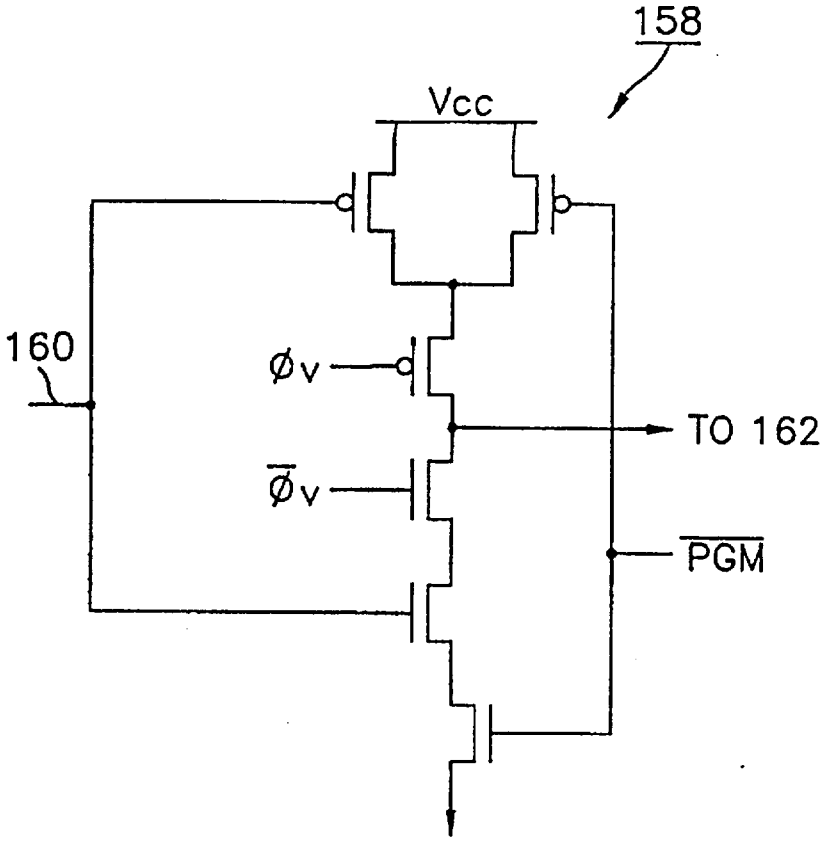
158
Vcc
160
ϕ_V
$\overline{\phi}_V$
TO 162
$\overline{PGM}$

FIG. 8b

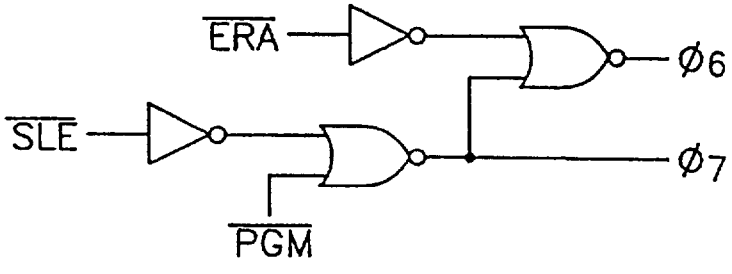
$\overline{ERA}$
$\overline{SLE}$
$\overline{PGM}$
ϕ_6
ϕ_7

FIG. 8c

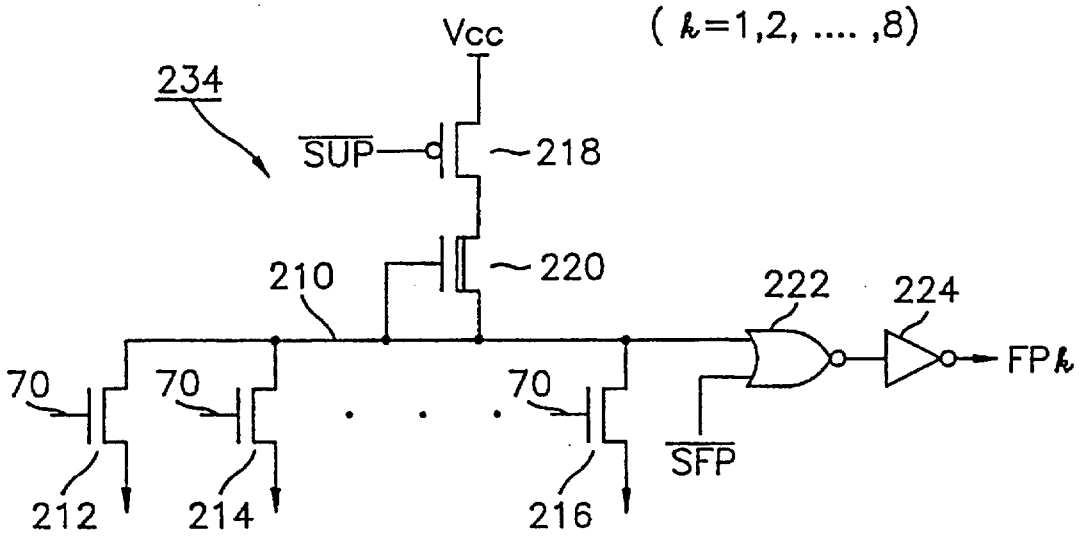

FIG. 9a

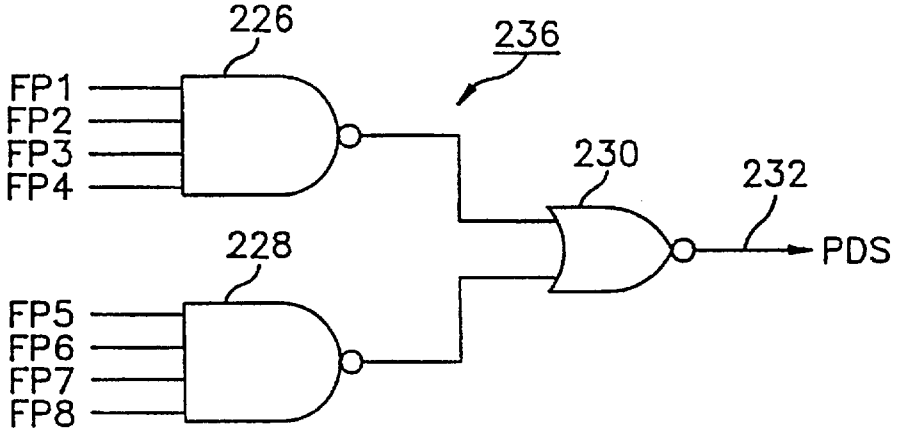

FIG. 9b

FIG. 9

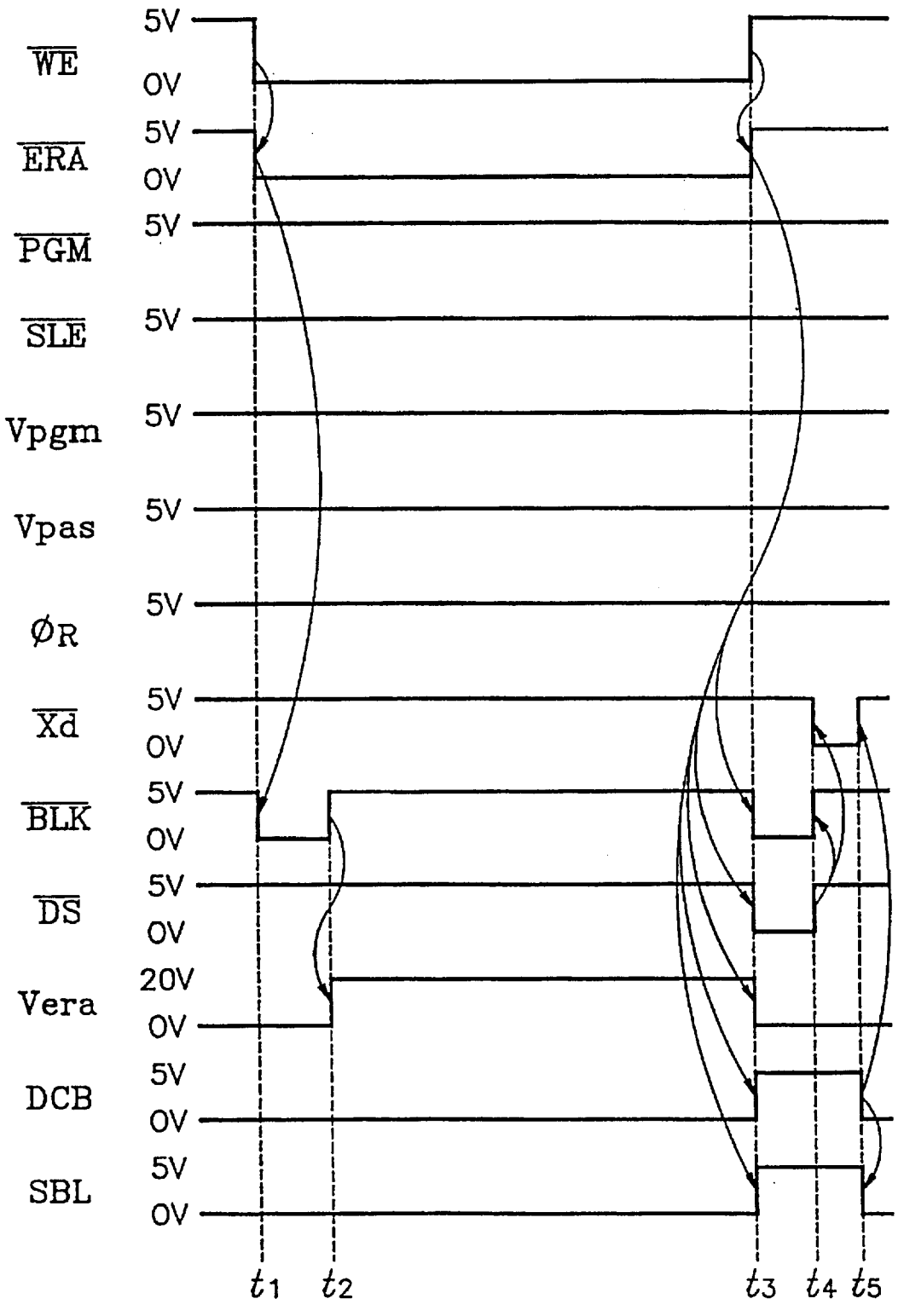
$\overline{WE}$
$\overline{ERA}$
$\overline{PGM}$
$\overline{SLE}$
Vpgm
Vpas
$\emptyset_R$
$\overline{Xd}$
$\overline{BLK}$
$\overline{DS}$
Vera
DCB
SBL
5V
0V
20V
t_1 t_2 t_3 t_4 t_5

FIG. 10

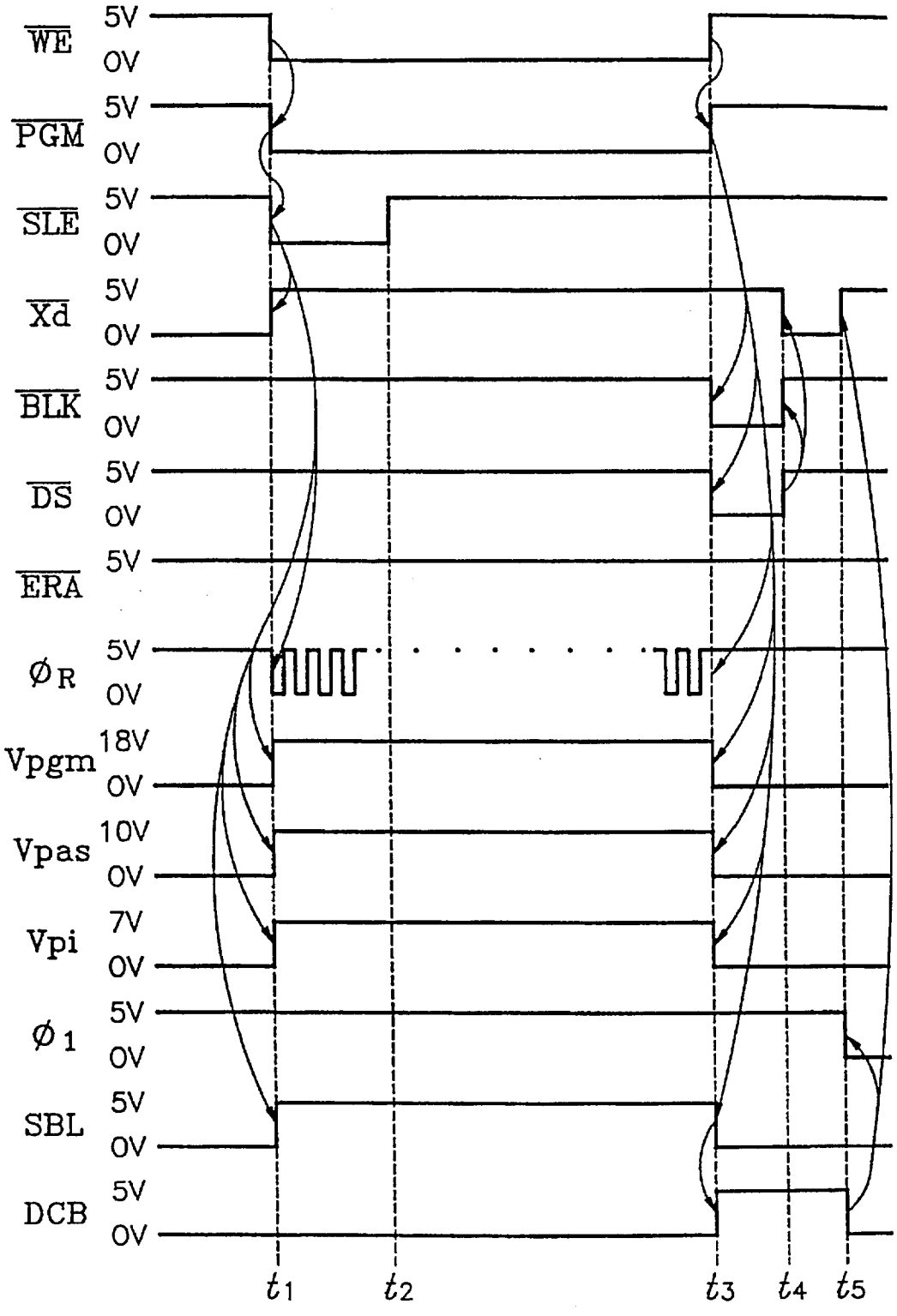
$\overline{WE}$
5V
0V
$\overline{PGM}$
5V
0V
$\overline{SLE}$
5V
0V
$\overline{Xd}$
5V
0V
$\overline{BLK}$
5V
0V
$\overline{DS}$
5V
0V
$\overline{ERA}$
5V
ϕ_R
5V
0V
Vpgm
18V
0V
Vpas
10V
0V
Vpi
7V
0V
ϕ_1
5V
0V
SBL
5V
0V
DCB
5V
0V
t_1
t_2
t_3
t_4
t_5

FIG. 11

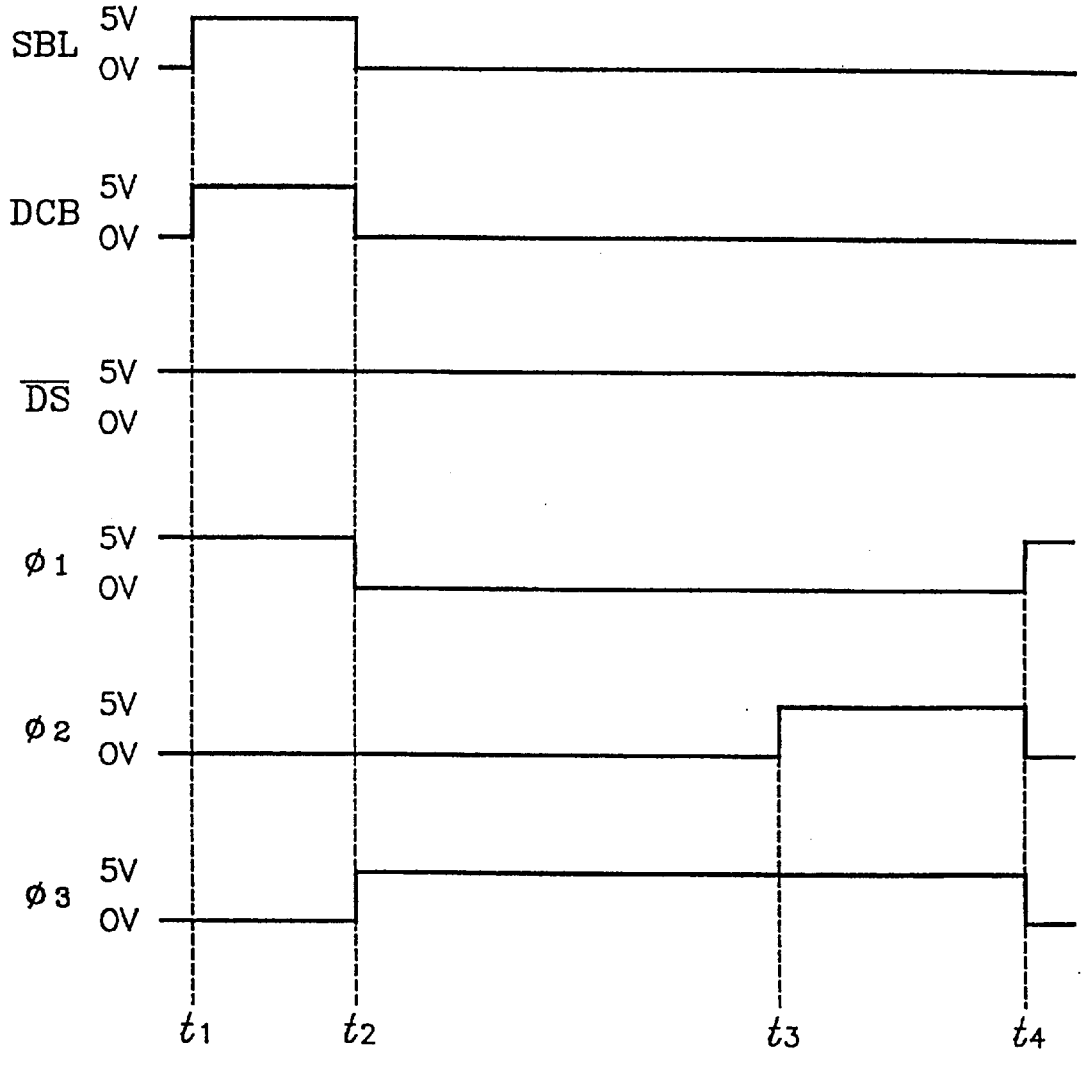
SBL
5V
0V
DCB
5V
0V
$\overline{DS}$
5V
0V
ø1
5V
0V
ø2
5V
0V
ø3
5V
0V
t1
t2
t3
t4

FIG. 12

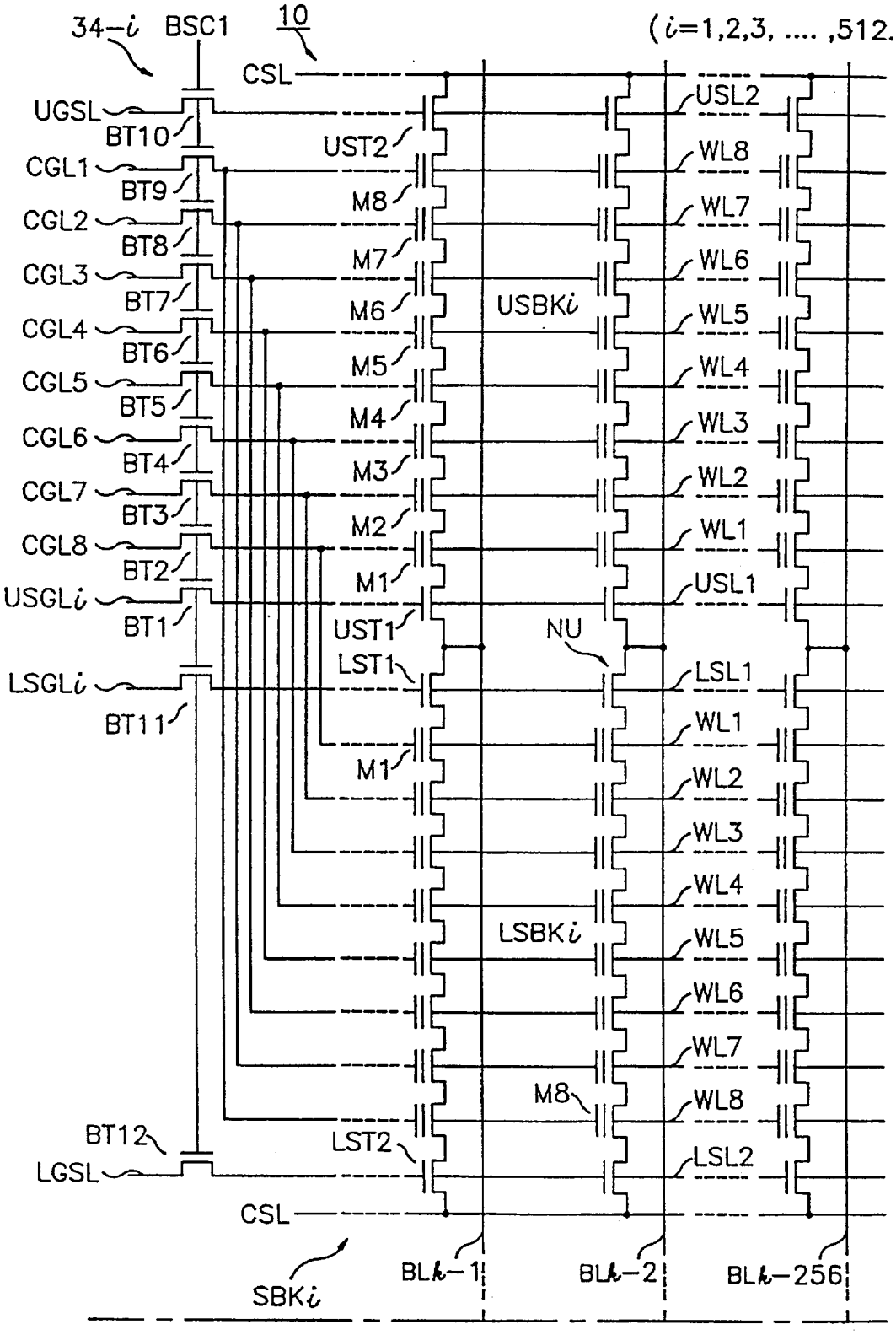
34-i
BSC1
10
(i=1,2,3, ... ,512.)
CSL
UGSL
BT10
UST2
USL2
CGL1
BT9
M8
WL8
CGL2
BT8
M7
WL7
CGL3
BT7
M6
WL6
USBKi
CGL4
BT6
M5
WL5
CGL5
BT5
M4
WL4
CGL6
BT4
M3
WL3
CGL7
BT3
M2
WL2
CGL8
BT2
M1
WL1
USGLi
BT1
UST1
USL1
NU
LST1
LSGLi
BT11
LSL1
M1
WL1
WL2
WL3
WL4
LSBKi
WL5
WL6
WL7
M8
WL8
BT12
LST2
LGSL
LSL2
CSL
SBKi
BLk-1
BLk-2
BLk-256

FIG. 13a

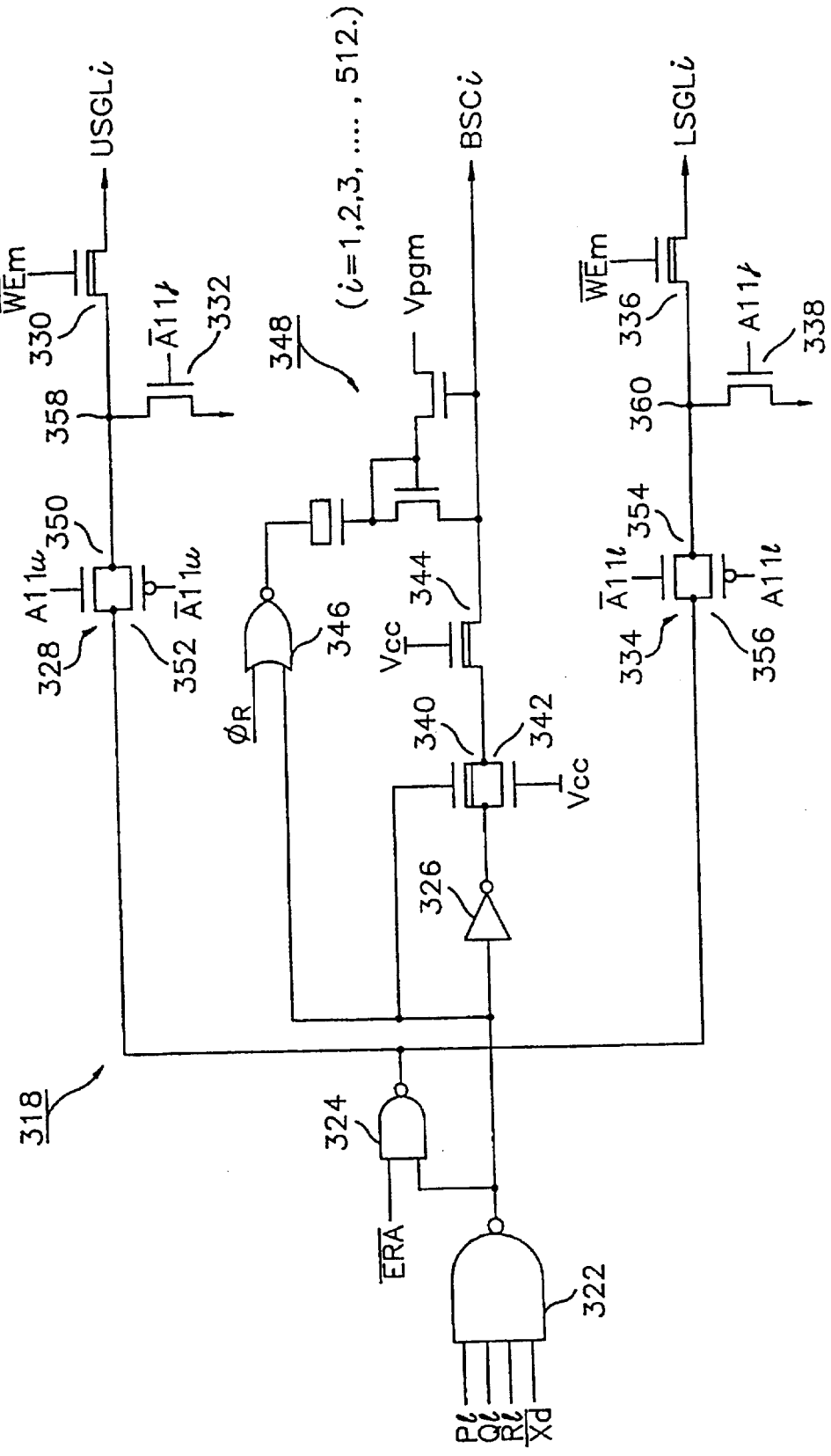
USGLi
BSCi
LSGLi
(i=1,2,3, ... , 512.)
Vpgm
WEm
A11
A11u
A11l
328
330
332
334
336
338
340
342
344
346
348
350
352
354
356
358
360
Vcc
ØR
318
324
326
ERA
322
Pi
Qi
Ri
Xd

FIG. 14

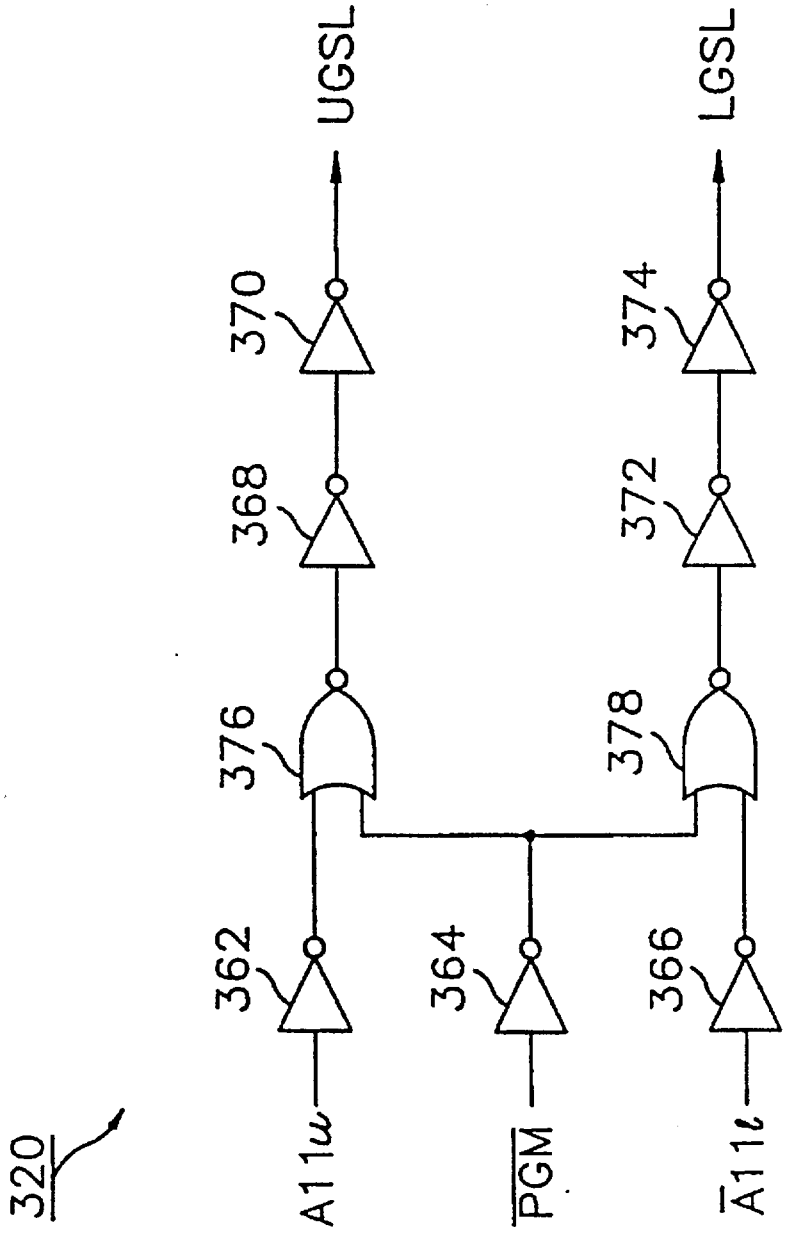

FIG. 15

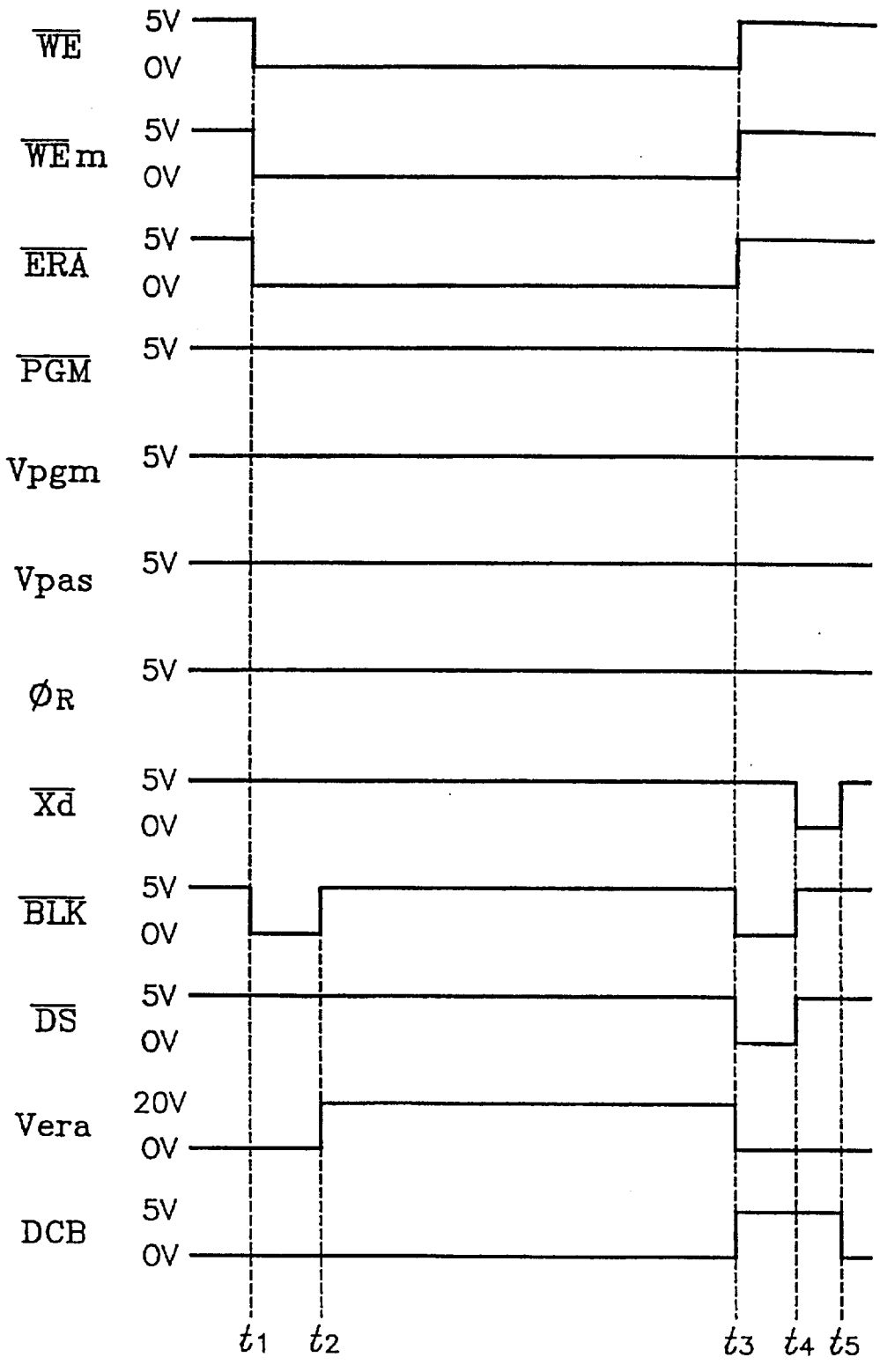
$\overline{WE}$
5V
0V
$\overline{WE}$m
5V
0V
$\overline{ERA}$
5V
0V
$\overline{PGM}$
5V
Vpgm
5V
Vpas
5V
$\emptyset_R$
5V
$\overline{Xd}$
5V
0V
$\overline{BLK}$
5V
0V
$\overline{DS}$
5V
0V
Vera
20V
0V
DCB
5V
0V
t_1
t_2
t_3
t_4
t_5

FIG. 16

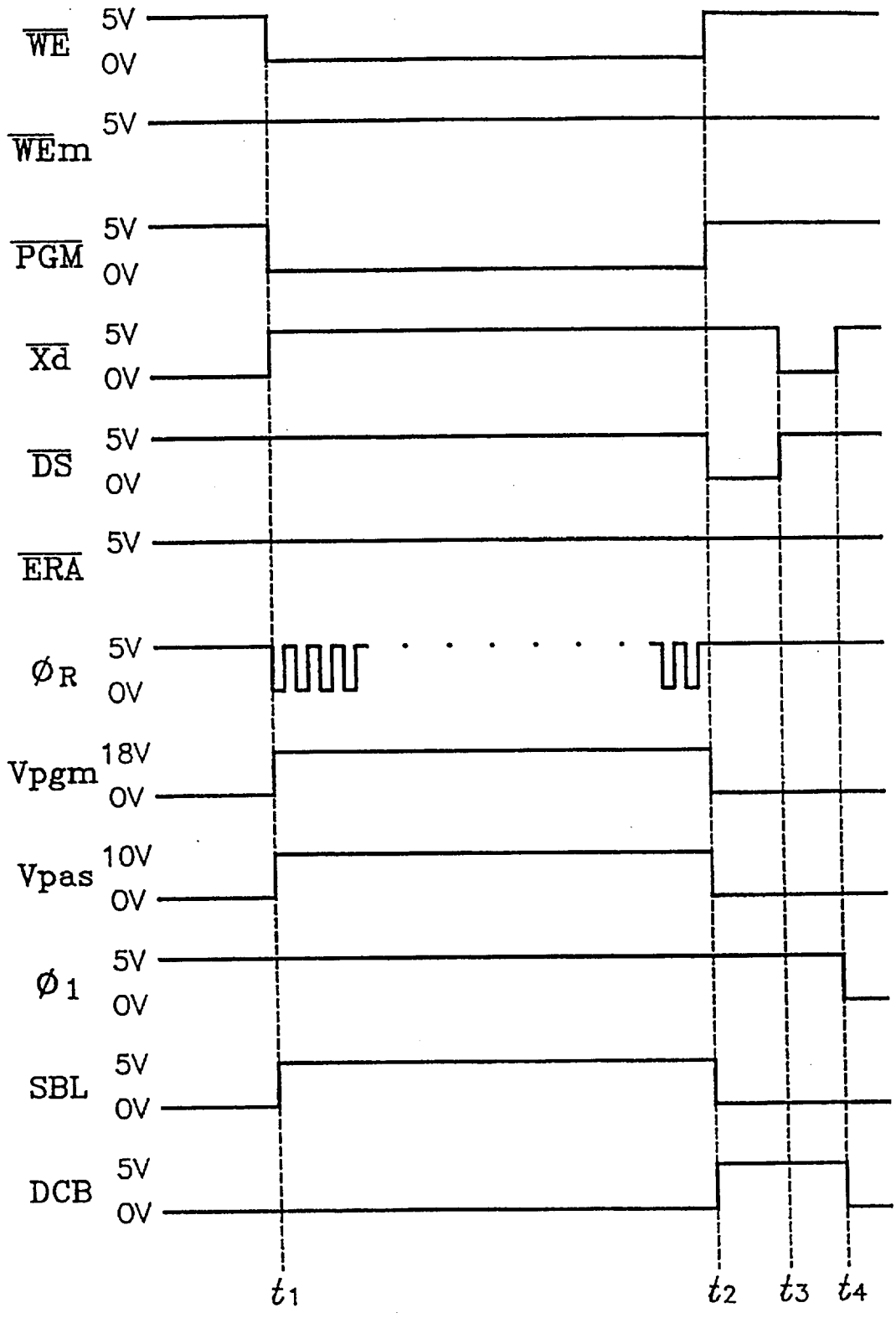
$\overline{WE}$
5V
0V
$\overline{WEm}$
5V
$\overline{PGM}$
5V
0V
$\overline{Xd}$
5V
0V
$\overline{DS}$
5V
0V
$\overline{ERA}$
5V
ϕ_R
5V
0V
Vpgm
18V
0V
Vpas
10V
0V
ϕ_1
5V
0V
SBL
5V
0V
DCB
5V
0V
t_1
t_2
t_3
t_4

FIG. 17

NONVOLATILE SEMICONDUCTOR MEMORY

This is a division of application Ser. No. 07/171,300, filed Dec. 22, 1993, now U.S. Pat. No. 5,473,563.

FIELD OF THE INVENTION

The present invention relates to electrically erasable and programmable nonvolatile semiconductor memories and, more particularly, but not exclusively, to electrically erasable and programmable nonvolatile semiconductor memories with NAND structured cells.

BACKGROUND OF THE INVENTION

Various systems controlled by recent computers or microprocessors require the development of an electrically erasable and programmable read-only memory (hereinafter referred to as a EEPROM) of a high density. Particularly, since the use of a hard disk with a rotary magnetic disk as a secondary storage occupies a relatively large area in a portable computer system such as a battery-powered computer system of notebook size, system designers take much interest in the development of EEPROMs of high density and high performance occupying a smaller area. To achieve a high density EEPROM, it is a major problem to reduce the area occupied by memory cells. To solve such a problem, an EEPROM has been developed which contains NAND structured cells being capable of decreasing the number of selection transistors per cell and contact holes coupled with a bit line. Such a NAND structured cell is disclosed in the IEDM, pp 412 to 415, 1988 under the title of "NEW DEVICE TECHNOLOGIES FOR 5V-ONLY 4 Mb EEPROM WITH NAND STRUCTURE CELL". This NAND structured cell (hereinafter referred to as a NAND cell unit or a NAND cell) is comprised of a first selection transistor whose drain is connected to the corresponding bit line via a contact hole; a second selection transistor whose source is connected to a common source line; and eight memory transistors whose channels are connected in series between the source of the first selection transistor and the drain of the second selection transistor. The NAND cell is formed on a p-type semiconductor substrate, and each memory transistor includes a floating gate layer formed on a gate oxide layer over a channel region between its source and drain regions and a control gate layer separated from the floating gate layer by an intermediate insulating layer. To program of write a selected memory transistor in the NAND cell, an operation of simultaneously erasing all memory transistors therein must be followed by the programming operation. The simultaneous erasure is performed by applying 0 volts to the bit line and raising the gate of the first selection transistor and control gates of all memory transistors to 17 volts. This causes all memory transistors to be changed into enhancement mode transistors which are assumed as binary logic "1" programmed transistors. To program a selected memory transistor to a binary logic "0" 22 volts are applied to the bit line, the gate of the first selection transistor and control gates of memory transistors between the first selection transistor and the selected memory transistor, while 0 volts are applied to the control gate of the selected memory transistor, control gates of memory transistor between the selected memory transistor and the common source line, and the gate of the second selection transistor. Thus, the selected memory transistor is changed into a depletion mode transistor by the Fowler-Nordheim tunneling (F-N tunneling) of holes from its drain to its floating gate. However, the problem of programming in this manner is that a portion of the gate oxide of the selected memory transistor is subjected to a stress induced by application of the high voltage to its drain, and the partially stressed gate oxide causes leakage current to flow. This results in degrading more and more the data retention capability of the memory cell according to an increase of the number of cycles of erasing and/or programming, thereby reducing the reliability of the EEPROM. To solve this problem, an improved device structure, in which the NAND cells are formed on a p-type well region imbedded in an n-type semiconductor substrate, and further improved erasing and programming technologies utilizing the improved device structure are disclosed in the symposium on VLSI Technology, pp 129 to 130, 1990 under the title of "A NAND STRUCTURED CELL WITH A NEW PROGRAMMING TECHNOLOGY FOR HIGHLY RELIABLE 5V-ONLY FLASH EEPROM".

Erasure of all memory transistors in this NAND cell is performed by applying 0 volts to all control gates and a high potential of 20 volts to the p-type well region and the n-type substrate, thereby uniformly extracting electrons from their floating gates to the well region. As a result, each memory transistor has a threshold voltage of about −4 volts which represents a state of depletion mode, i.e. a logic "0". To program a selected memory transistor in the NAND cell, a high voltage of 20 volts is applied to the gate of the first selection transistor and the control gate of the selected memory transistor, while 0 volts are applied to the gate of the second selection transistor, and an intermediate voltage of 7 volts is applied to control gates of unselected memory transistors. If the selected memory transistor is to be written or programmed into a logic "1", 0 volts are applied to the bit line connected with the NAND cell, thereby injecting electrons into the floating gate of the selected memory transistor. This results in causing the selected memory transistor to become enhancement mode. On the contrary, if the selected memory transistor is to be programmed to a logic "0", a program inhibition voltage of 7 volts instead of 0 volts is applied to the bit line to inhibit the programming of the selected memory transistor. Since such a programming operation uniformly injects electrons from the p-type well to its floating gate via its gate oxide layer, the partial stress on the thin gate oxide layer does not occur to a significant degree, and the gate oxide leakage current may thus be prevented.

However, when the memory capacity becomes high, such ways of uniform erasing and programming cause problems in the case that system designers want to erase a portion or a block of previously written or programmed memory cells in order to reprogram. In this case, a conventional approach is to simultaneously erase all memory transistors in a memory cell array, i.e. to carry out a flash erasure, and then to newly reprogram the content of all programs. Thus, since significantly reusable portions or blocks of the memory array are simultaneously erased, the reprogramming not only needs a long time, but also is inconvenient. It may be appreciated that such problems seriously occur when the memory density becomes more higher. To solve these problems, it is made possible only to erase all memory transistors in a selected memory block. However, in the case of an EEPROM using the above-mentioned improved erasing and programming techniques, to prevent the erasing of all memory transistors in an unselected block, it is required that a high voltage equal to an erase voltage or a high voltage of about 18 volts or more be placed on their control gates.

Thus, this technology has a drawback that a decoding circuit for performing a block erasing operation becomes complicated in design. In addition, when the density of the EEPROM cells increases, an on-chip occupying area of the decoder increases, thereby making it difficult to design the decoder.

Another problem area of the prior art is that of programming. To prevent the programming of non-programmed memory transistors, which must maintain previous data, of memory transistors on a selected word line, it is required that each of the bit lines corresponding to the non-programmed memory transistors be raised to the intermediate, i.e. the program inhibiting voltage, via a charge pump circuit connected thereto. In addition, when the memory capacity is increased, the number of bit lines or the length of each bit line is increased. Consequently, it is necessary that a high voltage generating circuit on the same chip for supplying the high voltages to the charge pump circuits has a high performance. Such a high voltage generating circuit and the charge pump circuits give a problem in increasing the area occupied by the on-chip peripheral circuits.

Conventional EEPROMs include a page program mode for high-speed programming. The page programming operation is composed of a data loading operation and a programming operation. The data loading operation comprises sequentially latching or storing data of a byte size from input/output terminals to a data register. The programming operation comprises simultaneously writing the data stored in the data register into memory transistors on a selected word line via bit lines. The page programming technology on an EEPROM with NAND cells is disclosed in the IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 25, NO. 2, pp 417 to 423, APRIL 1990.

Conventional EEPROMs employ a programming verification technique to enhance their reliability. The verification means checking to determine if programmed cells are programmed so as to have desired threshold voltages. Technologies of the programming verification may be classified into an external verification technique controlled by a microprocessor and an internal verification technique performed by an on-chip verification circuit. The external verification technique is disclosed in the IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 26, NO. 4, pp 492 to 495, April 1991 and U.S. Pat. No. 5,053,990. The external verification technique has a problem in that it takes a predetermined long time to determine if programmed cells are well programmed. In addition, whenever reprogramming is performed after the failure of the programming, it is necessary that the data loading operation is performed again. However, the internal verifying technique has an advantage that the programming verification is performed at a higher speed. The internal verifying technique is disclosed in Korean Patent Laid Open NO. 91-17445 and U.S. PAT. NO. 4,811,294. In these documents, the verification is performed in such a manner that comparator means compare data stored in a data register with data read out in pages from memory cells via sense amplifiers. However, such a scheme employing comparator means increases the area occupied by on-chip peripheral circuits.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a nonvolatile semiconductor memory with NAND structured cells which can reduce the size of chip.

It is another object of the present invention to provide a nonvolatile semiconductor memory with NAND structured cells which can reduce power consumption.

It is further object of the present invention to provide a nonvolatile semiconductor memory which performs an erasing of selected one of memory blocks.

It is still further object of the present invention to provide a nonvolatile semiconductor memory which is programmable without application of a program inhibition voltage of high voltages on unselected bit lines in order to reduce a chip size and power consumption.

It is another object of the present invention to provide methods for block erasing and programing which are capable of reducing on-chip occupying area and power consumption in a nonvolatile semiconductor memory with NAND structured cells.

It is another object of the present invention to provide a nonvolatile semiconductor memory in which on-chip area of peripheral circuits can be reduced in size.

It is further object of the present invention to provide a nonvolatile semiconductor memory in which over programming can be prevented.

According to an aspect of the present invention, a nonvolatile semiconductor memory includes, word lines formed over a surface of a semiconductor substrate; cell units arranged on said surface to form an array, each said unit including at least one memory transistor which has source and drain regions formed in said substrate but separated by a channel region, a charge storage layer formed over the channel region, and a control gate formed over the floating gate and coupled to a corresponding one of said word lines, said array being divided into a plurality of memory blocks each having a certain number of cell units; and means, responsive to an address in a data erase mode, for applying an erase voltage to said substrate, and simultaneously floating word lines of memory blocks unselected by said address, whereby erasure of memory transistors of said unselected memory blocks is prevented by capacitive coupling of a predetermined amount of said erase voltage to the word lines of said unselected memory blocks.

According to another aspect of the present invention, a nonvolatile semiconductor memory includes, a semiconductor substrate having a well region; memory transistors formed on the well region and arranged in a matrix form of rows and columns, the memory transistors comprising cell units each of which has a predetermined number of memory transistors connected in series, and first and second terminals at its both ends, cell units in respective rows constituting a memory block, each memory transistor having source and drain regions formed in the well region but separated by a channel region, a floating gate formed over the channel region to store charge representing binary data, and a control gate formed over the floating gate; word lines each being connected to control gates of memory transistors in a corresponding row; bit lines generally intersecting the word lines; a common source line; first and second selection lines generally in parallel with the word lines; first selection transistors respectively connected between first terminals of cell units in each memory block and corresponding bit lines for selectively connecting therebetween, gates of first selection transistors associated with each memory block being connected to a corresponding first selection line; second selection transistors connected between second terminals of cell units in each memory block and the common source line for selectively connecting therebetween, gates of second selection transistors associated with each memory block being connected to a corresponding second selection line; data register connected to the bit lines for providing binary data to the bit lines, the register providing logic high level

voltages to bit lines associated with memory transistors programmed to one binary data of the binary data while providing reference voltages to bit lines associated with memory transistors programmed to the other binary data thereof; and control means connected to the word lines and the first and second selection lines for applying a program voltage to a selected one of word lines of a selected memory block and pass voltages to unselected word lines of the unselected memory block while applying a logic high level voltage to the first selection line associated with the selected memory block and rendering nonconductive second selection transistors associated therewith, whereby channel regions and source and drain junctions of memory transistors in the selected memory block are capacitively charged to program inhibition voltages.

According to another aspect of the present invention, a method for programming memory transistors in a row in a semiconductor memory which comprises a semiconductor substrate; memory transistors formed on a surface of the substrate and arranged in rows and columns, the memory transistors comprising cell units each of which has a predetermined number of memory transistors connected in series, and first and second terminals at its both ends, each memory transistor having source and drain regions formed in the substrate but separated by a channel region, a floating gate formed over the channel region to store binary data, and a control gate formed over the floating gate, cell units in respective rows constituting a memory block; word lines each being connected to control gates of memory transistors in a corresponding row; bit lines generally intersecting the word lines, the first terminal of each of cell units of each memory block being connected to a corresponding one of the bit lines via a first selection transistor; and a common source line connected to the second terminal of each of cell units via a second selection transistors, the method includes the steps of applying a program voltage to a selected word line of a selected memory block and a pass voltage lower than the program voltage to the remaining word lines thereof, while applying a logic high level voltage lower than the .pass voltage to gates of first selection transistors associated with the selected memory block and rendering nonconductive second selection transistors associated therewith, the logic high level voltage corresponding to a logic high state; and applying a logic low level voltage corresponding to a logic low state to bit lines associated with memory transistors programmed from one binary data to the other binary data, while applying the logic high level voltage to bit lines associated with memory transistors not programmed, whereby channel regions and source and drain junctions of the nonprogrammed memory transistors are capacitively charged to a voltage level between the logic high level voltage and the program voltage so as to prevent programming, while those of the programmed memory.

BRIEF DESCRIPTION OF DRAWING

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

FIG. **1** shows a schematic block diagram of an electrically erasable and programmable read-only memory according to the present invention;

FIG. **2** is comprised of FIGS. **2***a* and **2***b*: FIG. **2***a* illustrating the arrangement of memory cells within first and second memory blocks associated with a k-th column block, and transfer transistor arrays connected thereto; and FIG. **2***b* showing an input/output buffer, a column decoder and selection circuit, a data register and sense amplifiers associated with the k-th column block;

FIG. **3** shows a plan view of a pattern for one of a plurality of NAND cells constituting a memory cell array;

FIG. **4** shows a cross-sectional view of the NAND cell taken substantially along line IV—IV of FIG. **3**;

FIG. **5** shows a schematic circuit diagram of a block selection control circuit used in an embodiment of FIG. **2**;

FIG. **6** shows a schematic circuit diagram of a control gate driving circuit used in embodiments of FIG. **2** and FIG. **13**;

FIG. **7** shows a schematic circuit diagram of a source line driving circuit used in the embodiment of FIG. **2**;

FIG. **8***a* shows a circuit diagram of a tristate inventer used in FIG. **2***b*;

FIG. **8***b* shows a circuit diagram of a tristate NAND gate used in FIG. **6**;

FIG. **8***c* shows a schematic timing circuit diagram for generating control signals ϕ_6 and ϕ_7 used in the block selection control circuit of FIG. **5**;

FIG. **9** shows a program determination circuit and is comprised of FIGS. **9***a* and **9***b*, in which FIG. **9***a* is a circuit diagram showing a portion of the program determination circuit and FIG. **9***b* is a circuit diagram showing a summation circuit;

FIG. **10** shows a timing chart of various control signals used in a block erasing mode according to a first embodiment of the present invention;

FIG. **11** shows a timing chart of various control signals used in a programming mode according to the first embodiment of the present invention;

FIG. **12** shows a timing chart of various control signals used in a programming verification mode and a reading mode according to the first and modified embodiments of the present invention;

FIG. **13** is a circuit diagram showing a schematic modified embodiment and is comprised of FIGS. **13***a* and **2***b*, in which FIG. **13***a* is a circuit diagram illustrating an arrangement of memory transistors within an i-th memory block having shared word lines in the k-th column block;

FIG. **14** shows a schematic circuit diagram of a block selection control circuit associated with the modified embodiment of FIG. **13**;

FIG. **15** shows a schematic circuit diagram of a ground line driving circuit associated with the modified embodiment of FIG. **13**;

FIG. **16** shows a timing chart of various control signals used in a block erasing mode of the modified embodiment; and

FIG. **17** shows a timing chart of various control signals used in a programming mode of the modified embodiment.

In the figures, like reference numerals denote like or corresponding parts.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following description, numerous specific details, such as memory cells, the number of NAND cells, the number of bit lines, the value of voltages, circuit elements and parts and so on, are set forth in order to provide a thorough understanding of the present invention. It will be

understood by those skilled in the art that other embodiments of the present invention may be practiced without these specific details, or with alternative specific details.

The term "memory transistor" as used herein refers to a floating gate MOS FET having a source, a drain, a floating gate and a control gate. The term "programming" is used to describe the writing of data into selected memory transistors. The term "NAND cell charging" is defined as the charging of the channel and the source and drain junction capacitors of respective memory transistors constituting the NAND cell to a predetermined potential.

In the following description, symbols k and i are respectively used for those parts associated with a k-th column block and an i-th memory block. Symbol j represents a notation associated with a j-th word line.

The term "ground potential" (or like terms such as "ground voltage" or "earth" potential or voltage" is used conveniently in this specification to denote a reference potential. As will be understood by those skilled in the art, although such reference potential may typically be zero potential, it is not essential that it is so, and may be a reference potential other than zero.

An example of an EEPROM of the present invention is fabricated by using CMOS manufacturing technologies on a common chip, in which depletion mode n-channel MOS transistors each having a threshold voltage of −2 to −3 volts (hereinafter referred to as D-type transistors), enhancement mode n-channel MOS transistors each having a threshold voltage of about 0.7 volts (hereinafter referred to as n-channel transistors) and p-channel MOS transistors each having a threshold voltage of about −0.9 volts (hereinafter referred to as p-channel transistors) are employed.

FIG. **1** illustrates a schematic block diagram of one example of an EEPROM according to the present invention.

FIG. **2** is composed of FIG. **2***a* and FIG. **2***b* in parallel relationship with each other, and shows, for the convenience of illustration, only those elements associated with the k-th input/output terminal I/Ok, a memory cell array **10**, input and output buffers **26** and **28**, a column decoder **30**, a column selection circuit **32**, a data register and sense amplifier **12** and a transmission transistor array **34**-i which is connected with the memory cell array **10** and constitutes a portion of a block selection control circuit **18**. It should be noted that elements associated with the remaining input/output terminals are identical to those associated with the terminal I/Ok.

Referring now to FIGS. **1** and **2**, the memory cell array **10** of the present EEPROM is composed of NAND cells NU arranged in a matrix form of 1,024 rows and 2,048 columns, and includes 1,024 memory blocks BK1 to BK1024 divided in a row direction. Each NAND cell is composed of memory transistors M1 to M8 whose drain-source paths are connected in series between the source of a first selection transistor ST1 and the drain of a second selection transistor ST2. Gates of the first and second selection transistors ST1 and ST2 and control gates of the memory transistors M1 to M8 are respectively connected to first and second selection lines SL1 and SL2 perpendicular to bit lines BLk-1 to BLk-256 (k=1,2, . . . ,8) and word lines WL1 to WL8. Thus, the memory transistors M1 to M8 are disposed at intersections of the word lines WL1 to WL8 and the bit lines BLk-1 to BLk-256. Drains of the first selection transistors ST1 are respectively connected with corresponding bit lines, and sources of the second selection transistors ST2 are connected to a common source line CSL. Consequently, the memory cell array **10** is comprised of memory cells of a total of 1,024×8×2,048 (=16,777,216), and each memory block is comprised of memory cells of a total of 8 ×2,048 (=16,384). The memory cell array **10** is divided into eight column blocks Bk (k=1,2, . . . ,8) respectively corresponding to input/output terminals I/01 to I/08, and each column block has 256 bit lines or column lines which are parallel in a column direction. Thus, each column block includes memory cells totalling 256 Kbit (=1,024×256).

The memory cell array **10** is formed on a p-well region in a semiconductor substrate. FIGS. **3** and **4** respectively show a plan view and a cross-sectional view of one of the NAND cells NU constituting the memory cell array **10**.

Referring to FIGS. **3** and **4**, the semiconductor substrate **72** is of a p-type silicon monocrystalline material which is cut on the (1,0,0) crystal orientation at an impurity concentration of about 7×10^{14} atoms/cm^3. A p-type well region **76** with an impurity concentration of about 2×10^{16} atoms/cm^3 is formed having a depth of about 4μm from a main surface **78** of the substrate **72**. The well region **76** is surrounded by a n-type well region **74** of about 10μm in depth with an impurity concentration of about 5×10^{15} atoms/cm^3. Heavily doped N^+ regions **80** to **92** are formed on the main surface **78** of the well region **76** and separated by each of a plurality of channel regions **94**. One part of the N^+ region **80** is a contact region connected via a contact hole **96** to a bit line BL of a metal material, such as an aluminum, which extends over an insulation layer **112**, and the other part of the N^+ region **80** also serves as a drain region of the first selection transistor ST1. The N^+ regions **82** to **90** serve as common source-drain regions of two adjacent transistors of transistors ST1, M1 to M8 and ST2. One part of the N^+ region **92** is a source region of the second selection transistor ST2, and the other part of the N^+ region **92** serves as buried common source line CSL. However, the line CSL may be a conductor layer which is insulatively formed within the insulating layer **112** contacting with the N^+ source region **92** of the transistor ST2 via a contact hole. Gate layers **98** and **100** of a refractory metal silicide material, such as a tungsten silicide, each of which has a thickness of about 1,500Å, are respectively formed on gate insulating layers **102** of about 300Å thickness, overlying channel regions of the first and second selection transistors ST1 and ST2.

Floating gate layers **104** of a polycrystalline silicon material are insulatively formed with a thickness of about 1,500Å on gate insulating layers **106** of about 100Å thickness overlying channel regions **94** of memory transistors M1 to M8, respectively. Control gates **108** of the same material and thickness as the gate layers **98** and **100** are respectively formed over the floating gate layers **104** interposing intermediate insulating layers **100**, such as ONO insulating layers of silicon dioxide-silicon nitride-silicon dioxide materials, of about 250Å thickness. The gate layers **98** and **100** and the control gate layers **108** are respectively shared by the first and second selection lines SL1 and SL2 and word lines WL1 to WL8, i.e. conductor layers which are fabricated from the same material as the gate and control gate layers **98**, **100** and **108**. The gate layers **98** and **100**, control gate layers **108**, floating gate layers **104**, the first and second selection lines SL1 and SL2, and word lines WL1 to WL8 are insulated from one another with an insulating layer **112** of insulating materials, such as a silicon dioxide and a BPSG or a PSG.

The bit line BL is connected with the contact region **80** via the contact hole **96** and extends in a column direction on the insulating layer **112**. The p-type well region **76** and the n-type well region **74** are connected to a well electrode **114** in common via contact holes (not shown). An erasing voltage is applied to the well electrode **114** in an erasing

operation, and a reference potential, i.e. ground potential, is applied to the well electrode **114** in operations except the erasing operation, i.e. in programming, programming verification and reading operations. However, the substrate **72** is always at the reference potential. The memory cell array **10** may also be formed on a p-type well region formed in an n-type monocrystalline silicon substrate.

Returning now to FIGS. **1** and **2**, the block selection control circuit **18** serves to select a predetermined memory block of the memory blocks BK1 to BK1024, and to provide control signals on control gate lines CGL1 to CGL8 from a control gate driving circuit **20** to word lines WL1 to WL8 in the selected memory block according to various operation modes, such as the erasing, programming, programming verification and reading modes. In FIG. **2***a*, illustration is made of transfer transistor arrays **34**-i constituting a portion of the block selection control circuit **18**. Each of the transfer transistor arrays **34**-i includes transfer transistors BT1 to BT10 for connecting the first and second selection gate lines SGLi-1 and SGLi-2 and control gate lines CGL1 to CGL8 to the first and second selection lines SL1 and SL2 and word lines WL1 to WL8, respectively.

According to one feature of the illustrated embodiment of the present invention, the block selection control circuit **18** renders nonconductive the transfer transistors associated with unselected memory blocks in an erasing operation, thereby causing word lines in unselected memory blocks to become floating. In a programming operation, the block selection control circuit **18** renders conductive the second transistor ST2 in a selected memory block, thereby charging the program inhibition voltage from a source line driving circuit **22** to channels and source and drain junctions of memory transistors in the selected memory block.

FIG. **5** shows a schematic circuit diagram for a block selection control circuit **18** connected to a transfer transistor array **34**-i of FIG. **2***a*. For example, in the case of i=2, lines SGL2-1, SGL2-2 and BSC2 of FIG. **5** are respectively connected to lines SGL2-1, SGL2-2 and BSC2 of the transfer transistor array **34**-2 associated with the second memory block BK2 as shown in FIG. **2***a*. Thus, it should be understood that though FIG. **5** shows, for the convenience of illustration, only a single circuit for selecting the i-th memory block BKi, the block selection control circuit of FIG. **5** corresponding to each of memory blocks BK1 to BK1024 resides on the present EEPROM chip as a peripheral circuit.

Referring now to FIG. **5**, NAND gate **120** is a row decoder for receiving address signals Pl, Ql and Rl and a reset signal Xd. The address signals Pl, Ql and Rl are signals predecoded by row address signals from a predecoder (not shown) for predecoding row address signals A_{11},$\overline{A_{11}}$ to A_{20}, $\overline{A_{20}}$ which are output from an address buffer for storing a row address a_{11} to a_{20} from external address input terminals. The row decoder **120** provides a logic low state of 0 volts (hereinafter referred to as an "L" state or an "L" level) on a line **122** when selected, and outputs a logic high state of 5 volts (hereinafter referred to as an "H" state or an "H" level) thereon when unselected. Two input terminals of NAND gate **124** are connected to the line **122** and a signal BLK, respectively. The signal BLK is a control signal for setting word lines WL1 to WL8 to the reference potential before or after the respective operations, as will be discussed hereinafter. The output of the NAND gate **124** is connected to the first selection gate line SGLi-1 and to the block selection control line BSCi via a current path of D-type transistor **126** for inhibiting the transfer of a high voltage. The gate of the transistor **126** is connected to a program control signal PGM for maintaining an "L" state in a programming operation. A charge pump circuit **128** is connected with the block selection control line BSCi for providing, when the line BSCi is selected, a program voltage V_{pgm} on the line BSCi by the pumping of a clock ϕ_R in the programming operation. The charge pump circuit **128** is a known circuit comprised of n-channel transistors **130** and **132** and a MOS capacitor **134**.

Two input terminals of NAND gate **136** are respectively connected with an erase control signal ERA and the line **122**. A transfer gate **148** composed of n-channel transistor **140** and p-channel transistor **142** is connected between the output of the NAND gate **136** and a connecting node **146**. The gate of n-channel transistor **140** is connected to a control signal ϕ_6, and the gate of p-channel transistor **142** is connected to the complement signal of ϕ_6 via an inverter **138**. The current path of n-channel transistor **144** is connected between the node **146** and the reference potential, and its gate is connected with a control signal ϕ_7. The source-to-drain current path of D-type transistor **150** for preventing the transfer of a high voltage is connected between the node **146** and the second selection gate line SGLi-2, and its gate is connected to a control signal WE. A charge pump circuit **152** having the same construction as the circuit **128** is connected to the second selection gate line SGLi-2 for providing a pass voltage V_{pas} thereon during the programming operation when the line SGLi-2 is selected.

FIG. **8***c* is a schematic circuit diagram for generating the control signals ϕ_6 and ϕ_7 as used in FIG. **5**. In an erasing operation or mode, ϕ_6 and ϕ_7 are all in "L" states, and in a NAND cell charging operation as will be discussed later, ϕ_6 is in "H" state and ϕ_7 is in "L" state. In programming verification and reading operations, ϕ_6 is in "H" state and ϕ_7 is in "L" state.

FIG. **6** illustrates one of eight control gate driving circuits, i.e. the j-th control gate driving circuit which constitutes control gate driving means and is associated with the j-th word line. The outputs of the control gate driving circuits are respectively connected to control gate lines CGL1 to CGL8 which are respectively connected to word lines WL1 to WL8 via transfer transistor arrays **34**-i. From the point of view of reduction of total chip size, it would be preferable that the control gate driving circuits be provided in common in an on-chip peripheral circuit so as to drive word lines of a selected memory block according to various operation modes.

Referring now to FIG. **6**, NAND gate **154** is a row decoder receiving row address signals $A_8/\overline{A_8}$, $A_9/\overline{A_9}$ and $A_{10}/\overline{A_{10}}$ from address buffer (not shown). The decoder **154** outputs "L" state upon selection of the line CGLj while outputting "H" state upon unselection thereof. The output of the decoder **154** and a control signal PVF are respectively connected to two input terminals of NOR gate **173**. An output signal ϕ_v of the NOR gate **173** and its complement signal $\overline{\phi_v}$ via an inverter **174** are provided to control a tristate NAND gate **158** and a verifying voltage generator **164**. The control signal PVF maintains an "L" state only in a programming verification operation. Thus, in every operation excepting the programming verification operation, the control signal PVF stays at "H" level, thereby causing the signal ϕ_v to be in an "L" state while causing the signal $\overline{100_v}$ to be in an "H" state. In the programming verification operation, if the line CGLj is selected, ϕ_v becomes "H" state and its complement $\overline{\phi_v}$ becomes "L" state while, if the line CGLj is unselected, ϕ_v becomes "L" state and ϕ_v becomes "H" state. NAND gate **156** inputs the output of the decoder **154** and control signals DS and ERA, respectively. Two input terminals of the tristate NAND gate **158** are respectively con-

nected to an output line **160** of the NAND gate **156** and the control signal PGM. The tristate NAND gate **158** illustrated in FIG. **8***b* is enabled in response to ϕ_v at "L" level and $\overline{\phi_v}$ at "H" level while becoming high impedance with ϕ_v at "H" level and $\overline{\phi_v}$ at "L" level. Thus, in the programming verification operation, the NAND gate **158** stays in the high impedance state only at the time when the line CGLj is selected. The output of the NAND gate **158** is connected to a connecting node **162** to which the verifying voltage generator **164** is connected.

The verifying voltage generator **164** is comprised of a p-channel transistor **166** and n-channel transistors **168, 170** and **172** whose current paths are connected in series between the power supply voltage Vcc and the reference potential. The gate of the p-channel transistor **166** is connected to a chip enable signal $\overline{CE}$, and gates of the transistors **168** and **170** are connected to the signal ϕ_v from the NOR gates **173**. Drain and gate of the transistor **172** are connected in common. The verifying voltage generator **164** is enabled by ϕ_v at "H" level only in the programming verification operation, thereby producing a verifying voltage of about 0.8 volts to the connecting node **162**. Connected between the connecting node **162** and the control gate line CGLj is the source-to-drain current path of D-type transistor **176** for inhibiting the transfer of a high voltage, the gate of which is connected to the control signal PGM.

Two input terminals of NAND gate **178** are respectively connected to the output of the NAND gate **156** and the clock ϕ_R from a ring oscillator (not shown). Between the output of the NAND gate **178** and the gate of a driving n-channel transistor **182** is connected a charge pump circuit **180** which has the same construction as the above-mentioned charge pump circuit. Drain and source of the transistor **182** are connected to the program voltage V_{pgm} and the control gate line CGLj, respectively. Inverter **190** receives the program control signal PGM, and the current path of D-type transistor **192** for preventing the transfer of a high voltage is connected between the output of the inverter **190** and the gate of the transistor **182** which is connected to the control signal PGM. As will be discussed hereinafter, a circuit **196** which is comprised of NAND gate **178**, the charge pump circuit **180** and the driving transistor **182** provides means for supplying the program voltage V_{pgm} to the control gate line CGLj when the line CGLj has been selected by row address signals $A_8/\overline{A_8}$, $A_9/\overline{A_9}$ and $A_{10}/\overline{A_{10}}$ in a program mode.

Two input terminals of NOR gate **188** are respectively connected to the output of the NAND gate **156** and the clock ϕ_R. Between the output of the NOR gate **188** and the gate of a driving n-channel transistor **184** is connected a charge pump circuit **186**. Drain and source of the transistor **184** are respectively connected to the pass voltage V_{pas} and the control gate line CGLj. Between a connecting node **202** and the gate of the transistor **184** is connected the current path of D-type transistor **194** for preventing the transfer of a high voltage, the gate of which is connected to the control signal PGM. As will be discussed hereinafter, a circuit **200** which is comprised of NOR gate **188**, the charge pump circuit **186** and the driving transistor **184** provides means for supplying the pass voltage V_{pas} to the control gate line CGLj when the line CGLj is selected by the row address signals in the program mode.

FIG. **7** shows a schematic circuit diagram of a source line driving circuit which is connected in common to the common source line CSL as shown in FIG. **2***a*. The source line driving circuit **22** is composed of an inverter **204** whose input terminal is connected to the control signal PGM, a D-type transistor **206** whose current path is connected between the output terminal of the inverter **204** and the common source line and whose gate is connected to the control signal PGM, and a charge pump circuit **208** connected to the common source line CSL. The charge pump circuit **208** serves to boost the common source line to a program inhibition voltage V_{pi} in the program mode.

The input/output buffer **16** is comprised of the input buffer **26** and the output buffer **28** which are each connected to input/output terminals. The input buffer **26** connected to each of input/output terminals I/O1 to I/O8 is a conventional circuit for converting a byte of data (8-bit data) therefrom to CMOS level data and temporarily storing it. Output buffers **28** are conventional circuits to simultaneously output 8-bit data read out from the corresponding column blocks to the corresponding input/output terminals.

The column decoder and selection circuit **14** of FIG. **2***b* is comprised of the column decoder **30** and the column selection circuit **32**. The column selection circuit **32** associated with each of the column blocks is comprised of transfer transistors T1 to T256, source-to-drain paths of which are respectively connected between a common bus line CBLk and lines DLk-1 to DLk-256. Gates of the transfer transistors T1 to T256 are respectively connected to parallel lines TL1 to TL256 which are connected to the column decoder **30**. The column decoder **30** selects one of the lines TL1 to TL256 in response to column address signals from address buffers (not shown), thereby rendering conductive transfer transistors connected with the selected line.

The data register and sense amplifier **12** is connected between the lines DLk-1 to DLk-256 and bit lines BLk-1 to BLk-256 which are associated with the corresponding column block, as shown in FIG. **2***b*. In series between the bit lines BLk-1 to BLk-256 and nodes **36** are respectively connected drain-to-source paths of D-type transistors **38** and **40**. Gates of the D-type transistors **38** are connected to the power supply voltage Vcc to prevent the transfer of high voltages induced on the bit lines BLk-1 to BLk-256 in a block erasing operation. Gates of the D-type transistors **40** are connected to a control signal ϕ_1 staying at "H" level of about 5 volts during programming. Between the nodes **36** and nodes **42** are respectively connected drain-to-source paths of n-channel transistors **44**. Gates of the transistors **44** are connected to a control line SBL staying at "H" level during programming. Between the nodes **42** and nodes **46** are respectively connected latches PBk-1 to PBk-256 constituting the data register which is referred to as a page buffer. Each of the latches is comprised of two inverters cross connected. The latches PBk-1 to PBk-256 serve not only as a page buffer for temporarily storing data so as to simultaneously write the data into memory cells via respective corresponding bit lines in a programming operation, but also as verifying detectors for determining if the program was well performed in a programming verification operation and as sense amplifiers for sensing and amplifying data on bit lines which is read out from memory cells in a reading operation. A tristate inverter **48** and an n-channel transistor **49** are connected in parallel between each of the nodes **42** and its corresponding one of the lines DLk-1 to DLk-256. Each tristate inverter **48**, which is referred to as a clocked CMOS inverter, is enabled by a control signal ϕ_4 at "H" level while becoming high impedance by the signal ϕ_4 at "L" level. Thus, each of the inverters **48** serves as a buffer amp, being enabled in programming verification and reading operations. N-channel transistors **49** whose gates are connected to a control signal ϕ_5 are transfer transistors for transferring input data to the corresponding latches PBk-1 to PBk-256 in a programming operation. The tristate inverter

48 which is used in the present embodiment is illustrated as a schematic circuit diagram in FIG. 8*a*. Between each of nodes 46 and the reference potential are serially connected current paths of n-channel transistors 50 and 52. Gates of the transistors 52 are connected to a control signal ϕ_2, staying at "H" level during a verification sensing period in a programming verification operation and during a read sensing period in a read operation. Gates of the transistors 50 are respectively connected to the nodes 36, and drain-to-source paths of n-channel transistors 37 are respectively connected between the nodes 36 and the reference potential. Gates of the transistors 37 are connected in common to a line DCB to which a control signal is applied to cause bit lines to be discharged after completion of erasing and programming operations and to reset the data register to "L" state, i.e. "0" data prior to a reading operation.

The data register and sense amplifier 12 includes a constant current source circuit 33, which is referred to as a current mirror, according to the present embodiment. The constant current source circuit 33 comprises a reference portion 64 which is enabled in programming verification and reading operations and disabled in erasing and programming operations; and current source portions 66 comprised of p-channel transistors 54 whose drain-to-source paths are respectively connected between gates of the transistors 50 and the power supply voltage Vcc. The reference portion 64 is comprised of p-channel transistors 56 and 58 and n-channel transistors 60 and 62 to serve as a reference for the current source transistors 54. Source-to-drain paths of the p-channel transistors 56 and 58 are connected in parallel between the power supply voltage Vcc and a line 68, and the gate of the p-channel transistor 58 is connected to the line 68. Drain-to-source paths of the n-channel transistors 60 and 62 are connected in series between the line 68 and the reference potential. The gate of the n-channel transistor 60 is connected to a reference voltage V_{ref} of about 2 volts. Gates of the transistors 56 and 62 are connected to a control signal ϕ_3, and gates of the current source transistors 54 are connected to the line 68. Thus, in programming verification and reading operations, the current source transistors 54 connected to the reference portion 64 which is enabled by the control signal ϕ_3 serve to provide a constant current of about 4μA to bit lines BLk-1 to BLk-256.

A programming determination circuit 24 of FIG. 1 is connected via lines 70 to lines DLk-1 to DLk-256 of FIG. 2*b* to serve to determine if every programmed memory transistor reaches the range of desired threshold voltages in a programming verification operation.

FIG. 9 shows a schematic circuit diagram of the programming determination circuit 24. It should be noted that the circuitry of FIG. 9*a* is a portion of the programming determination circuit 24 associated with the k-th column block CBk, and eight circuits corresponding to the respective ones of column blocks present as a peripheral circuit on the on-chip EEPROM. A circuit shown in FIG. 9*b* is a summation circuit to perform a summation function for providing an "L" level when any one of signals FP1 to FP8 is "L" level. Referring to FIG. 9*a*, drain-to-source paths of n-channel transistors 212 to 216 are connected in parallel between a line 210 and the reference potential, and gates of the transistors 212 to 216 are respectively connected to lines 70 of FIG. 2*b*. Current paths of p-channel transistors 218 and D-type transistor 220 are connected in series, and the gate of the transistor 218 is connected to a control signal SUP staying at "L" level in a programming verification operation while the gate of the transistor 220 is connected to the line 210. The transistors 212 to 220 constitute a NOR gate 234. Two input terminals of NOR gate 222 are respectively connected to the line 210 and a control signal SFP which becomes "L" state only upon a verifying check. The input of an inverter 224 is connected to the output of the NOR gate 222, and the output terminal of the inverter 224 outputs FPk. The summation circuit 236 of FIG. 9*b* is comprised of NAND gate 226 connected to lines FP1 to FP4; NAND gate 228 connected with signals FP5 to FP8; and NOR gate 230 connected to outputs of the NAND gates 226 and 228.

Referring now to the timing charts of FIG. 10 to FIG. 12, an explanation will be given of operations and features of the first embodiment shown in FIGS. 1 to 9.

Block Erasing Mode

In a block erasing mode, the data register and sense amplifier 12, the column decoder and selection circuit 14, the input/output buffer 16 and the programming determination circuit 24 are all in off states. Explained in more detail, the column decoder 30 of FIG. 2*b* is reset, thereby rendering transfer transistors T1 to T256 nonconductive. Control signals ϕ_1 to ϕ_5 and signals on lines DCB and SBL are held in "L" states, so that the data register and sense amplifier 12 become nonconductive. The control signal SUP of FIG. 9*a* is held in "H" state, and the programming determination circuit 24 is thereby nonconductive. The source line driving circuit 22 provides "L" state, i.e. the reference potential of 0 volts on the common source line CSL by PGM staying at "H" level.

Now, an explanation will be given in conjunction with the timing chart of FIG. 10, assuming that simultaneous block erasing is performed on data stored in memory transistors in the memory block BK1.

The time interval between t_1 and t_2 is a period for discharging all word lines WL1 to WL8 to the reference potential. During this period, NAND gate 124 of FIG. 5 retains "H" level with the control signal BLK at "L" level, and D-type transistor 126 is conducting with PGM at "H" level. Thus, the block selection control line BSCi stays at "H" level of 5 volts. At this time, the charge pump circuit 128 is in a nonconducting state. Consequently, in this period, all of the block selection control lines BSC1 to BSC1024 maintain the potential of 5 volts. On the other hand, in this period, since control signals PVF and PGM stay at "H" levels and the control signal ERA is at "L" level, the outputs of NAND gate 156 and tristate NAND gates 158 remain at "H" level and "L" level, respectively. At this time, the tristate inverter 164 is in a high impedance state. Thus, the control gate line CGLj stays at "L" level of 0 volts via turned-on D-type transistor 176. Consequently, all of the control gate lines CGL1 to CGL8 maintain "L" level during this period. Transfer transistors BT1 to BT10 are all turned on by the potential of the block selection control lines BSC1 to BSC1024 of 5 volts, and word lines WL1 to WL8 are all discharged to the reference potential.

The time duration between t_2 and t_3 is a period to erase all memory cells in only a selected memory block. At time t_2, the decoder 120 receives address signals Pl, Ql and Rl which are all at "H" levels to select the memory block BK1, and the output of the decoder 120 thereby goes to "L" level. Thus, the output of NAND gate 124 goes to "H" level. Consequently, the block selection control line BSC1 corresponding to the selected memory block BK1 remains at the potential of 5 volts during the period between t_2 and t_3. However, decoders 120 associated with unselected memory blocks BK2 to BK1024 output "H" levels since at least one

of the address signals Pl, Ql and Rl is "L" level. Consequently, block selection control lines BSC2 to BSC1024 associated with the unselected memory blocks go to the reference potential of 0 volts. Thus, transfer transistors in the transfer transistor array 34-1 are all turned on, and word lines WL1 to WL8 in the memory block BK1 thereby go to the reference potential. However, since the transfer transistor arrays 34-2 to 3-1024 connected with unselected memory blocks BK2 to BK1024 are all turned off, word lines associated therewith go to floating states.

At time t_2, the erase voltage Vera of about 20 volts is applied to the p-type well region 76 and the n-type well region 74 via the well electrode 114 of FIG. 4. During the time interval between t_2 and t_3, i.e. during the time period of about 10 msec, floating gates of memory transistors in the selected memory block BK1 accumulate holes by means of the F-N tunneling which is generated by the application of the erase voltage Vera to their channel, source and drain regions and that of the reference potential to their control gates. Thus, all of the memory transistors in the memory block BK1 are changed into D-type transistors having threshold voltages of about −3 volts. That is, all memory transistors in the memory block BK1 are erased to binary zero data.

However, in the case when the erase voltage V_{era} is applied to the p-well and N-well regions 76 and 74 via the well electrode 114 at time t_2, since word lines in unselected memory block BK2 to BK1024 are then in floating states, the word lines are thereby charged to substantially the erase voltage Vera by a capacitive coupling. Thus, the charged voltage of the word lines in the unselected memory blocks sufficiently reduces the electric field between the channel region and the control gate of each memory transistor such that its erasure can be prevented. The inventors have discovered that word lines in unselected memory blocks were charged to an amount of 80 to 90 percent of the erase voltage V_{era}, and data of programmed memory transistors in the unselected memory blocks was not destroyed or disturbed. Thus, in the block erasing of the present embodiment, since it is unnecessary to apply the program inhibition voltage from a voltage boosting circuit to word lines in unselected memory blocks, a reduction of the area occupied by the chip as well as the prevention of power consumption the area can effectively be accomplished. Moreover, the present invention has an advantage of increasing effective memory array area whilst reducing peripheral circuit area on a chip surface of a fixed size. This results in increasing the memory capacity of the EEPROM.

In the above-mentioned block erasing operation, the erase voltage applied to the well electrode 114 is coupled as well on the floated word lines as on floated bit lines. Thus, the bit lines are also charged to the erase voltage of about 20 volts in the block erase operation. To prevent voltage-induced stress on transistors 40 of FIG. 2*b* due to the charged erase voltage, D-type transistors 38, whose gates are connected to the power supply voltage Vcc, are respectively connected between bit lines BLk-1 to BLk-256 and the transistors 40.

During the block erasing operation between t_2 and t_3, the first selection line SL1 of the selected memory block BK1 maintains a potential of about 4.3 volts, and the second selection line SL2 of the block BK1 is in a floating state since control signals ϕ_6 and ϕ_7 are at "L" levels, thereby rendering transistors 140 to 144 of FIG. 5 nonconductive. The floating state of the second selection line SL2 thereof prevents current flowing via the line SL2 from the well electrode 114 when one or some of the second selection transistors ST2 thereof failed. During the block erasing operation, the voltage relationship of significant portions of selected and unselected memory blocks can be summarized in the following TABLE 1.

TABLE 1

	Voltage States For Selected Memory Block	Voltage States For Unselected Memory Blocks
First Selection Line SL1	4.3 V	0 V
Word Lines WL1 to WL8	0 V	Approximately 20 V
Second Selection Line SL2	Floating	Floating
Well Electrode	20 V	20 V

Turning to FIG. 10, the time duration between t_3 and t_5 is a period to discharge the charged voltage on bit lines and word lines. At time t_3, the block erasing operation terminates and the erase voltage Vera goes, to the reference potential while control signals WE and ERA go to "H" level. Between t_3 and t_4, the output of NAND gate 156 stays at "H" level with the control signal DS at "L" level. Thus, the output of NAND gate 158 goes to "L" level with the control signal PGM at "H" level. Consequently, control gate lines CGL1 to CGL8 maintain "L" levels between t_3 and t_4. During this period, the output of NAND gate 124 of FIG. 5 stays at "H" level with the control signal BLK at "L" level. Thus, each of the block selection control lines BSC1 to BSC1024 goes to a potential of 5 volts. Consequently, all transfer transistors BT1 to BT10 are turned on, and all word lines WL1 to WL8 are discharged to the reference potential. On the other hand, the first and second selection lines SL1 and SL2 are also discharged to a potential of 5 volts.

At time t_3, the line DCB goes to "H" level and ϕ_1 also goes to "H" level. Thus, the erase voltage charged on bit lines discharges to "L" level via transistors 37 shown in FIG. 2*b*.

At time t_4, control signals BLK and DS go to "H" levels and $X_d$goes to "L" level. Thus, NAND gate 120 of FIG. 5 goes to "H" level, and the first and second gate lines SGLi-1 to SGLi-2 and block selection control lines BSCi go to the reference potential.

Program Mode

The present EEPROM performs a data loading operation to store data input via input/output terminals into data latches PBk-1 to PBk-256 prior to a programming operation after an erasing operation.

Data loading operation is accomplished prior to a time t_1 of FIG. 11. During the data loading operation, control signals Xd, $\phi 2$, ϕ_3 and ϕ_4, program voltage V_{pgm}, pass voltage V_{pas}, p-well region 76, program inhibition voltage V_{pi} and lines SBL and DCB stay at "L" levels, and control signals WE, PGM, SLE, BLK, DS, ERA, PVF, SUP ϕ_R, ϕ_5 and ϕ_1 are at "H" levels. As can be seen in FIG. 5, since Xd is "L" level and BLK, ERA, SLE, WE and PGM are all "H" levels, block selection gate lines BSC1 to BSC1024 stay at "L" levels, thereby rendering transfer transistor arrays 34-1 to 34-1024 nonconductive. With the line SBL at "L" level, connection of data latches PBk-1 to PBk-256 to bit lines BLk-1 to BLk-256 is inhibited. The constant current circuit 33 and tristate inverters 48 of FIG. 2*b* are in nonconducting states with signals ϕ_3 and ϕ_4 at "L" levels.

Address inputting to external address input terminals is composed of row address a_8 to a_{20} and column address a_0 to a_7. The row address a_8 to a_{20} inputs to select one of memory blocks and one of the word lines during the data loading

operation so as to write data on all bit lines into memory cells at one time, i.e., the perform a page program in the programming operation after the completion of the data loading operation. The column address a_0 to a_7 is address signals having 256 cycles during the data loading operation. The column decoder **30** of FIG. **2***b* responds to the column address of 256 cycles based on the toggling of external write enable Signal WE_x to render transfer transistors T1 to T**256** conductive in sequence. At the same time, input buffer **26** corresponding to the respective column blocks sequentially outputs data input to the corresponding input/output terminal in response to the toggling of WE_x. Thus, output data from the respective input buffers **26** is stored in sequence into data latches PBk-**1** to PBk-**256** via sequentially turned-on transfer transistors T1 to T**256** and corresponding transfer transistors **49**.

After the above-mentioned data loading operation, the programming operation is started. One characteristic feature of the present embodiment is that the programming operation includes the NAND cell charging operation.

For the convenience of explanation of the programming operation, it is assumed that data stored in the data latches is to be written into memory transistors M_4 connected to a word line WL**4** in the memory block BK**1**.

The programming operation is performed during the time period between t_1 and t_3 as shown in FIG. **11**. During this period, p-well region **76**, signals WE, PGM, ϕ_2, ϕ_3, ϕ_4 and ϕ_5 and the line DCB stay at "L" levels while signals Xd, BLK, DS, ERA and ϕ_1 and the line SBL are all at "H" levels. The clock ϕ_R, the program voltage V_{pgm} (=18 volts), the pass voltage V_{pas} (=10 volts) and the program inhibition voltage V_{pi} (=7 volts) are supplied during this period. On the other hand, the row address a_8 to a_{20}, which is inputted during the above-mentioned data loading operation, is latched in the address buffer (not shown). Address signals Pl, Ql and Rl which are generated by predecoding address signals A_{11}, $\overline{A_{11}}$ to A_{20}, $\overline{A_{20}}$ of the latched address, are input to the decoder **120** of FIG. **5**. Address signals A_8,$\overline{A_8}$ to A_{10},$\overline{A_{10}}$ of the latched address are input to the decoder **154** of FIG. **6**.

At time t_1, the control signal Xd goes to "H" level, and address signals Pl, Ql and Rl selecting the memory block BK**1** are input to the NAND gate **120** of FIG. **5**. Then, the output of the gate **120** goes to "L" level, and outputs of NAND gates **124** and **136** go to "H" levels. Thus, the first selection gate line SGLi-**1** goes to a potential of 5 volts, and the block selection control line BSC**1** is boosted to the program voltage V_{pgm} of 18 volts by the pumping operation of the charge pump circuit **128**. On the other hand, the second selection gate line SGL**1**-**2** is boosted to the pass voltage V_{pas} of 10 volts by the pumping operation of the charge pump circuit **152** with "H" level transferred via transfer transistors **140**, **142** and **150**. Each decoder **120** associated with unselected memory blocks BK**2** to BK**1024** goes to "H" level, and the output of each NAND gate **124** corresponding thereto goes to "L" level. Thus, unselected block selection control lines BSC**2** to BSC**1024** go to a reference potential of 0 volts.

At time t_1, the program control signal PGM goes to "L" level and the common source line CSL, which is the output line of the source line driving circuit **22** of FIG. **7**, is boosted to the program inhibition voltage V_{pi}. That is, if PGM goes to "L" level, the common source line CSL goes to the absolute value, for example 2 to 3 volts, of the threshold voltage of D-type transistor **206** and is thereby boosted to the program inhibition voltage V_{pi} by means of the charge pump circuit **208**.

As previously mentioned, since address signals A_8,$\overline{A_8}$ to A_{10},$\overline{A_{10}}$ selecting the word line WL**4** were input to the decoder **154** of FIG. **6** in the previous data loading operation, the output of the decoder **154** associated with CGL**4** is at "L" level, and the outputs of the decoders **154** associated with unselected word lines WL**1** to WL**3** and WL**5** to WL**8** are at "H" levels. Thus, the output of NAND gate **156** associated with the selected word line WL**4** is at "H" level, and the output of NAND gates **156** associated with the unselected word lines are at "L" levels. At time t_1, the clock ϕ_R is generated. Then, NAND gate **178** and NOR gate **188** associated with the selected word line WL**4** respectively output the clock ϕ_R and "L" level, thereby providing the program voltage Vpgm on the selected control gate line CGL**4**. On the contrary, NOR gates **188** associated with unselected word lines output the clock ϕ_R, thereby providing the pass voltage V_{pas} on unselected control gate lines CGL**1** to CGL**3** and CGL**5** to CGL**8**.

At time t_1, the line SBL goes to "H" level. Thus, transfer transistors of FIG. **2***b* are all turned on so as to transfer data stored in latches PBk-**1** to PBk-**256** to corresponding bit lines BLk-**1** to BLk-**256**. All memory transistors of the selected memory block BK**1** in the previous block erase mode were erased to "L" levels, i.e. logic "0" data. In the data loading operation after a block erasing mode, latches corresponding to memory transistors which are to write "H" levels, i.e. logic "1" data were stored to "L" level, i.e. logic "0" data while latches corresponding to memory transistors which are to write logic "0" data were stored to logic "1" data. For the convenience of explanation, assume that logic "1" data is written into a memory transistor **240** which is connected to the selected word line WL**4** and bit line BL**1**-**2** of memory block BK**1** in the first column block CB**1** of FIG. **2***a* while logic "0" data is written into the remaining memory transistors connected to the word line WL**4** thereof. Then, the latch PB**1**-**2** has already stored logic "0" data while the remaining latches have already stored logic "1" data in the data loading operation. Thus, after time t_1, the conduction of transfer transistors **44** causes the bit line BL**1**-**2** to go to "L" level and the remaining bit lines to go to "H" levels of 5 volts.

Consequently, during the time duration between t_1 and t_2, the transfer transistor array **34**-**1** of FIG. **2***a* is conducting, and the first and second selection lines SL**1** and SL**2** in the selected memory block BK**1** respectively maintain 5 volts and V_{pas} (=10 volts) while the selected word line WL**4** and unselected word lines WL**1** to WL**3** and WL**5** to WL**8** maintain V_{pgm} (=18 volts) and V_{pas}, respectively. During the programming operation, since the common source line CSL maintains the program inhibition voltage V_{pi} (=7 volts), the second selection transistor ST**2** and memory transistors M**1** to M**8** in the block BK**1** are all turned on, and the first selection transistor **242** connected to the bit line BL**1**-**2** is turned on while remaining first selection transistors excluding the transistor **242** in the block BK**1** are turned off. Thus, current paths of memory transistors in the NAND cell including the memory transistor **240** are connected with the bit line BL**1**-**2**, and channels of the memory transistors and the respective junction capacitor of their sources and drains are thereby discharged to a reference potential of 0 volts. However, first selection transistors ST**1** associated with memory transistors which are to write logic "0" data are turned off, and channels of memory transistors in the NAND cells associated therewith and the respective junction capacitors of their sources and drains are charged to the program inhibition voltage V_{pi} (=7 volts). Thus, during the time period of about 100 μsec between t**1** and t**2**, a NAND cell

charging operation associated with memory transistors which are programmed to logic "0" data is carried out.

Turning to FIG. **11**, the time duration between t_2 and t_3, i.e. the period of about 2 msec, is a period to perform substantial programming. At time t_2, the signal SLE goes to "H" level and, as can be seen in FIG. **8***c*, ϕ_6 goes from "H" level to "L" level while ϕ_7 goes from "L" level to "H" level. Thus, transistors **144** of FIG. **5** are turned on, thereby causing all of second gate lines SGLi-2 to be connected with the reference potential. Thus, all of second selection transistors ST2 in the selected memory block BK1 are turned off. During this period, the program voltage V_{pgm} of about 18 volts is applied on the word line WL4 in the selected memory block BK1, and source, drain and channel of the memory transistor **240** are applied to 0 volts. Thus, the floating gate of the transistor **240** is accumulated with electrons by the F-N tunneling, thereby causing the transistor **240** to be changed into an enhancement mode transistor having a threshold voltage of about 0.8 volts. However, since junction capacitors of sources and drains of memory transistors excepting the transistor **240** and their channels are charged to the program inhibition voltage V_{pi}, injection of electrons into floating gates of these transistors is inhibited and these transistors remain as depletion mode transistors storing logic "0" data. That is, NAND cells associated with memory cells which are programmed to logic "0" data are blocked from connection to corresponding bit lines by the above-mentioned NAND cell charging, thereby being prevented from writing.

As discussed above, the voltage relationship of significant portions during the NAND cell charging and the programming operation can be summarized in the following TABLE 2.

TABLE 2

	Voltage States During NAND Cell Charging Period	Voltage States During Programming Period
First selection Line SL1 Of Selected Memory Block	5 V	5 V
Unselected Word Lines Of Selected Memory Block	V_{pas} = 10 V	V_{pas} = 10 V
Selected Word Line Of Selected Memory Block	V_{pgm} = 18 V	V_{pgm} = 18 V
Second Selection Line SL2 Of Selected Memory Block	V_{pas} = 10 V	0 V
Common Source Line CSL	V_{pi} = 7 V	V_{pi} = 7 V
Well Electrode	0 V	0 V

The time period between t_3 and t_5, i.e. the period of 500 nsec, is a period to discharge the boosted voltage on the bit lines and the word lines. At time t_3, control signals WE and PGM and the line DCB go to "H" levels, and control signals BLK and DS, voltages V_{pgm}, V_{pas} and V_{pi} and the line SBL go to "L" levels of 0 volts. The clock ϕ_R stops pulsing to be fixed at "H" level at the time t_3. On the other hand, during this period, ϕ_1 maintains "H" level and ϕ_2 and ϕ_3 maintain "L" levels. Thus, the source line driving circuit **22** outputs the reference potential on the common source line CSL. Control gate lines CGL1 to CGL8 of FIG. **6** go to a potential of 0 volts, and block selection control lines BSC1 to BSC1024 of FIG. **5** go to a potential of 5 volts. This results in causing all word lines to be discharged to the reference potential. At time t_4, Xd goes to "L" level and BLK and DS go to "H" levels. Thus, during the time period between t_4 and t_5, block selection control lines BSCi and first and second selection gate lines SGLi-1 and SGLi-2 go to the reference potential. On the other hand, since the line DCB and the signal ϕ_1 are at "H" levels during the time period between t_3 and t_5, the boosted voltages on the bit lines are discharged to the reference potential via transistors **37**. At time t_5, the signal ϕ_1 goes to "L" level.

Programming Verification Mode

The programming verification mode is performed immediately after the programming mode. The programming verification operation of the present invention is similar to the reading operation as will be discussed later. The difference as compared with the reading operation is that the voltage applied to a selected word line is a minimum threshold voltage which is to be written into memory transistors. This minimum threshold voltage will be referred to as a programming verification voltage. It is assumed that the programming verification voltage is 0.8 volts in the present embodiment.

The programming verification operation is carried out immediately after time t_5 in FIG. **11**, and a timing chart of the programming verification operation is of the time period between t_2 and t_4 as shown in FIG. **12**. At the initiation of the programming verification, i.e. at time t_5 of FIG. **11** or time t_2 of FIG. **12**, control signals Xd, ϕ_3 and ϕ_4 go to "H" levels and signals ϕ_1, PVF and SUP and the line DCB go to "L" levels. Thus, during the programming verification operation, control signals WE, PGM, SLE, Xd, BLK, DS, ERA, ϕ_3 and ϕ_4 and the clock ϕ_R maintain "H" levels, and voltages V_{pgm}, V_{pas} and V_{pi}, lines SBL and DCB and control signals ϕ_1, ϕ_5, PVF and SUP maintain "L" levels.

It is now assumed that the programming verification operation is performed to determine if a memory transistor **240** of FIG. **2***a* which was written to a logic "1" data in the previous programming mode was programmed with a desired minimum threshold voltage.

Where a command for executing a programming verification after completion of programming operation is input to EEPROM from the microprocessor via input/output terminals or other terminals or where a programming verification operation is automatically carried out after a programming operation, data stored into latches PBk-1 to PBk-256 in the programming operation is succeeded without reset by the programming verification operation. Thus, at the beginning of the programming verification operation, the latch PB1-2 is storing logic "0" data and the remaining latches are storing logic "1" data.

At time t_2 of FIG. **12**, the control signal Xd goes to "H" level and the decoder **120** of FIG. **5** then outputs "L" level in response to address signals Pl, Ql and Rl designating the memory block BK1. Then, since ϕ_6 and ϕ_7 respectively maintain "H" level and "L" level, first and second selection lines SGLi-1 and SGL1-2 and the block selection control line BSC1 go to "H" levels of 5 volts.

At time t_2, the control signal PVF goes to "L" level and address signals $A_8/\overline{A_8}$ to $A_{10}/\overline{A_{10}}$ designating the word line WL4 are fed to the decoder **154** of FIG. **6**. Then, NAND gate **158** becomes of high impedance and the verifying voltage generator **164** provides the verifying voltage of 0.8 volts on the control gate line CGL4. However, each decoder **154** associated with unselected word lines WL1 to WL3 and WL5 to WL8 output "H" levels. Then, the verifying voltage generator **164** becomes high impedance and NAND gate **158** outputs "H" level. Thus, control gate lines CGL1 to CGL3 and CGL5 to CGL8 go to "H" level of 5 volts. On the other hand, since PGM maintains "H" level at t_2, the source line

driving circuit **22** of FIG. **7** provides the reference potential on the common selection line CSL.

Consequently, the transfer transistor array **34-1** of FIG. **2***a* is conductive and the first and second selection lines SL1 and SL2 and unselected word lines WL1 to WL3 and WL5 to WL8 go to the potential of 5 volts while the selected word line WL4 goes to the potential of 0.8 volts. Thus, transistors connected with the selection lines SL1 and SL2 and the unselected word lines are turned on.

At time t_2, the control signal ϕ_3 goes to "H" level, thereby causing the constant current circuit **33** of FIG. **2***b* to be enabled. Thus, the constant current transistors **54** supply constant current of about 4μA to bit lines via connecting nodes **36** and transistors **40** and **38**.

Assume that the programmed memory transistor **240** has failed to program, i.e. the threshold voltage of the transistor **240** was below the program verifying voltage of 0.8 volts. Then, the transistor **240** is turned on and the bit line BL1-2 connected thereto goes to the reference potential of 0 volts. Since all transistors of NAND cells in the memory block BK1 which are connected with bit lines excluding the bit line BL1-2 are turned on, the bit lines also go to the reference potential. The period of time when word lines WL1 to WL8 and bit lines are established to the predetermined voltages in such a manner is a period of about 2μsec between t_2 and t_3 of FIG. **12**.

The time period between t_3 and t_4 of FIG. **12**, i.e. the period of about 500 nsec, is for verification sensing. The control signal ϕ_2 goes to "H" level at time t_3, and transistors **52** of FIG. **2***b* are thereby turned on. The transistor **50** whose gate is connected with the bit line BL1-2 via transistors **38** and **40** is turned off by the reference potential on the bit line BL1-2, thereby causing the latch PB1-2 to maintain logic "0" data. Similarly, since other bit lines are also at the reference potential, transistors **50** associated with these bit lines are turned off and latches excepting the latch PB1-2 thereby maintain previously stored logic "1" data. Verification sensing data stored in the latches PBk-1 to PBk-256 by the above-mentioned verification sensing operation is connected to gates of transistors **212** to **216** of FIG. **9***a* via turned-on inverters **48** and lines **70**. Thus, the "L" level verification sensing data stored in the latch PB1-2 is supplied via corresponding inverter **48** to the gate of transistor **214** which constitutes NOR gate **234** of FIG. **9***a* associated with the first column block CB1, thereby rendering the transistor **214** conductive and causing the line **210** to be discharged to the reference potential. Consequently, since the signal SFP goes to "L" level only when the programming verification is checked, FP1 goes to "L" level. However, since latches in other column blocks CB2 to CB8 store "H" levels, transistors **212** to **216** of NOR gate **234** corresponding to each one of the blocks CB2 to CB8 are in nonconductive states. Thus, each line **210** maintains "H" level by means of pull-up transistors **218** and **220** and FP2 to FP8 thereby stay at "H" levels. Thus, the output line **232** of the summation circuit **236** of FIG. **9***b* goes from "H" level to "L" level. This represents that the memory transistor **240** was undesirably programmed. That is, it is checked that the threshold voltage of the memory transistor **240** did not reach at a preset minimum threshold voltage. A program determination signal PDS on the line **232** is connected to a timing circuit (not shown) which generates timing signals between t_1 and t_5 as shown in FIG. **11** so as to perform a reprogramming in response to the signal PDS being at "L" level. That is, reprogramming operation is automatically performed. It would be noted that the reprogramming operation of the present embodiment may automatically be performed by the internal circuit of the present EEPROM without request of either reprogramming control or reloading of data from a microprocessor. However, if necessary, the microprocessor may control the reprogramming operation in response to the signal PDS from one of the input/output terminals of the present EEPROM chip.

Assuming that the memory transistor **240** reached the desired threshold voltage of 0.8 volts by the reprogramming operation, then the transistor **240** is in a nonconductive state during the programming verification operation performed after the reprogramming operation. Thus, the bit line BL1-2 is charged to the potential of about 2 to 3 volts by the constant current supplied via the constant current transistor **54**, thereby rendering conductive the transistor **50** connected with the bit line BL1-2. Consequently, the verification sensing data of latch PB1-2 is changed from logic "0" data to logic "1" data. As previously discussed, other latches are storing logic "1" verification sensing data. Thus, all of the latches PBk-1 to PBk-256 store logic "1" verification sensing data. That is, if all memory transistors were well programmed in the page programming operation, verification sensing data stored in the latches is changed into logic "1". Then, transistors **212** to **216** constituting NOR gates **234** of FIG. **9***a* are all turned off, and signals FP1 to FP8 go to "H" levels with the signal SFP at "L" level during the check of programming verification. Consequently, the summation circuit **236** of FIG. **9***b* outputs the program determination signal PDS, which is at "H" level. This represents that the programming operation had successfully been performed.

Now assume that some of memory transistors programmed with logic "1" had successfully been programmed and the remainder had unsuccessfully been programmed. Then, during the followed programming verification operation, latches corresponding to the former memory transistors are changed so as to store logic "1" data, while latches corresponding to the latter memory transistors maintain logic "0" data. Since latches in the former case are storing logic "1" data, their corresponding bit lines are charged to the potential of 5 volts during the followed reprogramming operation. However, in the same manner as the abovementioned programming operation, since, in the reprogramming operation, a selected first selection line stays at 5 volts and junctions of sources and drains of memory transistors and their channels are charged to the program inhibition voltage of 7 volts, first transistors connected with the charged bit lines on the selected first selection line are in nonconductive states. Thus, during the reprogramming operation, the successfully programmed memory transistors are prevented from programming by the charged program inhibition voltages. However, in the case of the latter, i.e. the unsuccessfully programmed memory transistors, since their corresponding latches are storing logic "0" data, reprogramming is performed only on them. With such repeating operations, if all memory transistors on a selected word line which are programmed with logic "1" data were successfully programmed, the program determination signal PDS outputs "H" level during the abovementioned programming verification operation, and the reprogramming operation is terminated. The present circuit used in the above-mentioned programming verification operation may also be applied to EEPROMs with NOR-type memory arrays.

The programming verification techniques as discussed above have various advantages as follows. First, the programming verification operation can automatically carried out by the internal circuit without the control of an external microprocessor. Second, since the data register is used as data latches in a data loading mode, verification sensing

circuits in a programming verification mode and sense amplifiers in a reading mode, as will be discussed hereinbelow, simplification of peripheral circuits may be accomplished. Third, the threshold voltages of programmed memory transistors may be tightly distributed within a narrow range above a preset minimum threshold voltage, and over-programming may be prevented. The tight distribution of threshold voltages can be accomplished by the execution of the programming operation within a shorter period, since successfully programmed memory transistors are automatically inhibited from programming due to the changed data of their corresponding latches.

Reading Mode

FIG. **12** illustrates a timing chart of the reading operation according to the present embodiment.

The time period between t1 and t2 in the drawing is a period to discharge word lines WL1 to WL8 and all bit lines BLk-1 to BLk-**256** to the reference potential and to reset so that latches PBk-**1** to PBk-**256** stores logic "0" data. During this period, the control signal ϕ_1 and lines SBL and DCB stay at "H" levels. Thus, bit lines BLk-**1** to BLk-**256** are discharged to the reference potential via the transistor **37** of FIG. **2***b*, and latches PBk-**1** to PBk-**256** are reset to logic "0" data by the conduction of transistors **37** and **44**. During the time period between t_1 and t_2, a timing chart of control signals WE, PGM, SLE, Xd, BLK, DS and ERA, the clock ϕ_R and voltages V_{pgm}, V_{pas} and V_{pi} is identical to the timing chart between t_3 and t_5 shown in FIG. **11**. Control signals PVF and SUP keep "H" levels during operations excepting the programming verification operation.

The time period between t_2 and t_4 is a period for sensing data read out from memory cells and storing the sensing data into latches PBk-1 to PBk-**256**. During the period, WE, PGM, SLE, Xd, BLK, DS, ERA, ϕ_3, ϕ_4 and ϕ_R maintain "H" levels, and V_{pgm}, V_{pas}, V_{pi}, lines SBL and DCB, ϕ_1 and ϕ_5 keep "L" levels.

An explanation will now be given, assuming that a reading operation is performed from memory transistors connected to the word line WL*4* in the memory block BK1 which was page programmed in the above-mentioned programming mode.

Operation between t_2 and t_3 is performed in a similar manner as the verification operation as discussed above. Thus, an explanation will be given in brief. The block selection circuit of FIG. **5** associated with the selected memory block BK1 makes first and second selection gate lines SGLi-1 and SGL1-2 and the block selection control lines BSC1 held at 5 volts in response to address signals Pl, Ql and Rl addressing the block BK1. Since the control signal PVF is at "H" level, the verifying voltage generator **164** of FIG. **6** is in a high impedance state and the NAND gate **158** is being enabled. Thus, the control gate line CGL*4* corresponding to the selected word line WL*4* is at the reference potential of 0 volts in response to address signals $A_8/\overline{A_8}$ to $A_{10}/\overline{A_{10}}$ designating the word line WL*4*. However, control gate lines CGL1 to CGL3 and CGL5 to CGL8 corresponding to unselected word lines WL1 to WL3 and WL5 to WL8 are at "H" levels of 5 volts. On the other hand, the source line driving circuit **22** of FIG. **7** outputs the reference potential on the common source line CSL. Consequently, the transfer transistor array **34**-1 of FIG. **2***a* is conductive, and first and second selection lines SL1 and SL2 and unselected word lines WL1 to WL3 and WL5 to WL8 in the block BK1 are thereby at 5 volts while the selected word line WL*4* therein is at 0 volts.

The control signal ϕ_3 goes to "H" levels at time t_2, thereby causing the current source circuit **33** to be enabled. Thus, the constant current transistors **54** supply the current of about 4μA onto bit lines BLk-1 to BLk-**256** via connecting nodes **36** and transistors **40** and **38**. Since only the memory transistor **240** is programmed with logic "1" the bit line BL1-2 is charged to about 2 to 3 volts and the remaining bit lines go to 0 volts. At time t_3 of FIG. **12**, the control signal ϕ_2 goes to "H" level, thereby rendering transistors **52** of FIG. **2***b* conductive. Then, only the transistor **50** associated with the bit line BL1-2 is turned on, thereby making the latch PB1-2 sense and store the logic "1". However, remaining latches continuously store logic "0" based on the previously mentioned reset operation since transistors **50** are turned off. That is, page reading is accomplished. Data stored in the latches PBk-**1** to PBk-**256** is output to input/output terminals I/O1 to **1/08** by a byte (8 bits) via inverters **48**, transfer transistors T1 to T**256** turned on in sequence in response to column address of 256 cycles and toggles of WE_x, and output buffer **28**.

Modified Embodiments

The EEPROM of the first embodiment explained in connection with FIG. **1** to FIG. **12** comprises the memory array including 1024 memory blocks each of which has NAND cells arranged in the same rows, and a source line driving circuit for generating the program inhibition voltage prior to the programming or reprogramming operation in order to charge it to the NAND cells. However, it should be noted that the present invention is not limited to such an embodiment. For example, the memory array used in other embodiments of the present invention may be comprised of memory blocks having shared word lines as discussed hereinafter. To charge the program inhibition voltage to NAND cell, a capacitive coupling way from control gates may be applied with no use of the source line driving circuit. This modified embodiment is illustrated in FIG. **13** to FIG. **17**.

FIG. **13** consists of FIG. **13***a* and FIG. **2***b*. FIG. **13***a* shows a memory array composed of memory blocks having shared word lines, and FIG. **2***b* shows the already discussed peripheral circuit connected with the memory array of FIG. **13***a*.

For simplification of the drawing, FIG. **13***a* shows only the arrangement of memory cells and shared word lines which are associated with the k-th column block in the i-th memory block SBKi. However, it should be noted that a memory array **10** having memory cells of 16 mega bits as shown in FIG. **13***a* is arranged in the same manner as the memory array of FIG. **2***a* excepting the shared word lines.

Referring to FIG. **13***a*, each of memory blocks SBKi (i=1, 2, 3, . . . , 512) is comprised of two submemory blocks, i.e. an upper memory block or a first submemory block USBKi and a lower memory block or a second submemory block LSBKi. Each of the upper and lower memory blocks USBKi and LSBKi has the same configuration as each of the memory blocks of FIG. **2***a*. Word lines WL1 to WL8 in the upper memory block USBKi are correspondingly connected with word lines WL1 to WL8 in the lower memory block LSBKi. That is, the upper memory block USBKi shares the word lines WL1 to WL8 with the lower memory block LSBKi.

The word lines WL1 to WL8 are respectively connected to control gate lines CGL1 to CGL8 via current paths of transfer transistors BT2 to BT9. A first upper selection line USL1 and a first lower selection line LSL1 are connected to

upper and lower selection gate lines USGLi and LSGLi via current paths of transfer transistors BT1 and BT11, respectively. Second upper and second lower selection lines USL2 and LSL2 are connected to upper and lower ground selection lines UGSL and LGSL via current paths of transfer transistors BT10 and BT12, respectively. Sources of second upper and lower selection transistors UST2 and LST2 are connected to a common source line CSL which is connected to the reference potential, i.e. the ground. Drains of first upper and lower selection transistors UST1 and LST1 are respectively connected to corresponding bit lines.

The control gate lines CGL1 to CGL8 are connected to the control gate driving circuit **20** explained in connection with FIG. **6**. Upper and lower selection gate lines USGLi and LSGLi are respectively connected to corresponding block selection control circuits **318** of FIG. **14**. Each of the block selection control circuits **318** serves to select one of upper and lower memory blocks in a selected memory block designated by address according to respective operation modes. It should be noted that the block selection control circuits **318** corresponding to the respective memory blocks SBKi are provided on the substrate of the on-chip EEPROM. Thus, it would be appreciated that two memory blocks substantially share one block selection control circuit since each block selection control circuit controls one memory block comprised of upper and lower memory blocks. This results in relatively increasing the area of memory array on the chip substrate of fixed size so as to increase the memory storage capacity since the chip occupying area of the peripheral circuit is decreased.

The upper ground selection line UGSL and the lower ground selection line LGSL are connected to a ground line driving circuit **320** illustrated in FIG. **15**. The ground line driving circuit **320** is a circuit connected in common with upper ground selection lines UGSL and lower ground selection lines LGSL in memory block SBKi. The ground line driving circuit **320** serves to provide proper voltages onto the upper and lower ground selection lines UGSL and LGSL according to the respective operation modes.

Referring to FIG. **14** showing the block selection control circuit which controls the i-th memory block SBKi, a decoder **322** receives address signals Pl, Ql and Rl and the control signal Xd. The address signals Pl, Ql and Rl are signals predecoded by address signals $A_{12}/\overline{A_{12}}$ to $A_{20}/\overline{A_{20}}$ of row address signals $A_{11}/\overline{A_{11}}$ to $A_{20}/\overline{A_{20}}$ from address buffer (not shown). The row address signal $A_{11}/\overline{A_{11}}$ is input to a timing circuit (not shown) in order to generate control signals A_{11u}, $\overline{A_{11u}}$, A_{111}, $\overline{A_{111}}$ and A_{11j}, $\overline{A_{11j}}$ for selecting one of either the upper memory block USBKi or the lower memory block LSBKi according to the respective operation modes. Logic states of these control signals according to the respective operation modes are given in the following TABLE 3, wherein "H" represents "H" level of 5 volts and "L" represents "L" level of 0 volts.

TABLE 3

	Upper Memory Block Selection A_{11} = H		Lower Memory Block Selection A_{11} = L	
	Erasing Mode	Reading, Programming And Programming Verification Mode	Erasing Mode	Reading, Programming And Programming Verification Mode
A_{11u}	H	H	H	L
$\overline{A_{11u}}$	L	L	L	H
A_{11j}	L	H	L	L
$\overline{A_{11j}}$	L	L	L	H
A_{111}	L	H	L	L
$\overline{A_{111}}$	H	L	H	H

The output of the decoder **322** is connected to one input terminal of NAND gate **324** and an input terminal of an inverter **326**. The other input terminal of NAND gate **324** is connected to the erase control signal ERA. The output of the NAND gate **324** is connected to the upper selection gate line USGLi via a CMOS transfer gate **328**, which consists of n-channel transistor **350** and p-channel transistor **352**, and the current path of D-type transistor **330**. Between a connecting node **358** and the reference potential is connected the current path of n-channel transistor **332**. Gates of N-channel transistors **350** and **332**, p-channel transistor **352** and D type transistor **330** are connected to control signals A_{11u}, $\overline{A_{11j}}$, $\overline{A_{11u}}$ and WE_m, respectively. The control signal WE_m is at "L" level during the block erasing operation and is at "H" level during remaining operations. The output of the NAND gate **324** is also connected to the lower selection gate line LSGLi via a CMOS transfer gate **334**, which consists of n-channel transistor **354** and p-channel transistor **356**, and the current path of D-type transistor **336**. The current path of n-channel transistor **338** is connected between a connecting node **360** and the reference potential. Gates of n-channel transistors **354** and **338**, p-channel transistor **356** and D-type transistor **336** are connected to control signals $\overline{A_{111}}$, A_{11j}, A_{111} and WE_m, respectively. The output of the inverter **326** is connected to the block selection control line BSCi via current paths of D-type transistor **340** and n-channel transistor **342**,.which are connected in parallel, and the current path of D-type transistor **344**. The gate of the D-type transistor **340** is connected to the output of the decoder **322**, and gates of the n-channel transistor **342** and the D-type transistor **344** are connected to the power supply potential Vcc of 5 volts. Two input terminals of NOR gate **346** are connected to the clock ϕ_R and the output of the decoder **322**, respectively. Between the output of the NOR gate **346** and the line BSCi is connected a charge pump circuit **348**.

If address signals selecting the memory block SBKi input to the block selection control circuit **318**, the block selection control line BSCi is at a potential of about 4.3 volts in erasing, programming verification and reading modes, and is at the program voltage V_{pgm} of 18 volts in a programming mode. On the contrary, the block selection control line of respective ones of block selection control circuits associated with unselected memory blocks is at the reference potential of 0 volts in all modes.

If the memory block SBKi is designated by the address signal and the address signal A11 is at "H" level, the upper selection gate line USGLi is at a potential of 5 volts in a programming, a programming verification and a reading modes, and the lower selection gate line LSGLi is at a potential of 0 volts by conduction of the transistor **338** in said modes. Similarly, if the memory block SBKi is addressed by the address signal and the address signal A_{11} is at "L" level, the lower selection gate line LSGLi is at a

TABLE 3-continued

	Upper Memory Block Selection A_{11} = H		Lower Memory Block Selection A_{11} = L	
	Erasing Mode	Reading, Programming And Programming Verification Mode	Erasing Mode	Reading, Programming And Programming Verification Mode
$\overline{A_{11j}}$	L	L	L	H
A_{111}	L	H	L	L
$\overline{A_{111}}$	H	L	H	H

potential of 5 volts in programming, programming verification and reading modes, and the upper selection gate line USGLi is at a potential of 0 volts by conduction of the transistor **332** in said modes. On the other hand, upper and lower selection gate lines USGLi and LSGLi are both in floating states of about 2 to 3 volts in a block erasing mode.

Referring to FIG. **15**, the ground line driving circuit **320** is comprised of inverters **362** to **374** and NOR gates **376** and **378**. The driving circuit **320** outputs 0 volts onto upper and lower ground selection lines UGSL and LGSL in a programming mode. If the upper memory block is selected in reading and programming verification modes, the upper ground selection line UGSL goes to "H" level of 5 volts, and the lower ground selection line LGSL goes to "L" level of **0** Volts. However, if the lower memory block is selected in reading and programming verification modes, the lower ground selection line LGSL goes to "H" level of 5 volts, and the upper ground selection line UGSL goes to "L" levels of 0 volts. On the other hand, upper and lower ground selection lines UGSL and LGSL go to "H" levels of 5 volts in a block erasing mode.

Operations of the modified embodiment are almost the same as those of the first embodiment, excepting operation to select either upper or lower memory block and operation to charge NAND cells by way of a capacitive coupling technique in a programming operation. Thus, a brief explanation of operation of the modified embodiment will be given, referring to the accompanying timing charts.

FIG. **16** shows a timing chart of the block erasing mode. In the drawing, the time period between t_1 and t_2 is for discharging all word lines in the memory array **10** to the reference potential of 0 volts. In this period, control gate lines CGL1 to CGL8 are at the reference potential as discussed in connection with FIG. **6**. During this period, BLK maintains "L" level, and the predecoder (not shown) generates address signals Pl, Ql and Rl being at "H" levels in response to the signal BLK. Thus, the decoder of FIG. **14** outputs "L" level. Consequently, block selection control lines BSC1 to BSC512 are all at the potential of about 4.3 volts, and transfer transistors BT2 to BT9 of transfer transistor arrays **34-1** to **34-512** of FIG. **13***a* are all turned on, thereby grounding all word lines.

The time period between t_2 and t_3 of FIG. **16** is for erasing a selected memory block. During the period, control gate lines CGL1 to CGL8 remain the reference potential identical to the case between t_1 to t_2. The block selection control circuit **318** of FIG. **14** associated with the selected memory block outputs the potential of about 4.3 volts onto a selected block selection control line. However, the block selection control circuits associated with unselected memory blocks output the reference potential onto unselected block selection control lines. Thus, word lines of upper and lower memory blocks in the selected memory block at time t_2 are all at the reference potential, and all of word lines in unselected memory block are in floating states. However, since the erase voltage V_{era} of 20 volts is applied to the well electrode **114** of FIG. **4** at time t_2, all word lines in the unselected memory blocks are capacitively coupled to about 20 volts, and data of memory transistors in the unselected memory blocks is not erased. However, during the time period between t_2 and t_3, every memory transistor in the selected memory block is changed into a D-type transistor having a threshold voltage of about −2 to −3 volts by the erase voltage which is applied between its channel and control gate. That is, logic "0" data is stored.

On the other hand, during the block erasing period between t_2 and t_3, since the selected block selection control line is at the potential of about 4.3 volts, and upper and lower selection gate lines USGLi and LSGLi are at about 2 to 3 volts, and upper and lower ground selection lines UGSL and LGSL are at 5 volts, the first upper and lower selection lines USL1 and LSL1 associated with the selected memory block are at about 2 to 3 volts and the second upper and lower selection lines USL2 and LSL2 associated with the selected memory block are in floating states. Thus, when any one of the second upper and lower transistors connected with the second upper and lower selection lines fails, the flow of leakage current is prevented via the second upper and lower selection lines USL2 and LSL2 from the well electrode **114**. During the block erasing operation, the voltage relationship of significant portions may be summarized in the following TABLE 4.

TABLE 4

	Selected Memory Block	Unselected Memory Block
First Upper And Lower Selection Lines USL1 And LSL1	Approximately 2–3 V	Floating
Word Lines WL1 to WL8	0 V	Approximately 20 V
Second Upper And Lower Selection Lines USL2 and LSL2	Floating	Floating
Well Electrode	20 V	20 V

The time period between t_3 and t_4 of FIG. **16** is for discharging word lines in unselected memory blocks to the reference potential. During this period, control gate lines CGL1 to CGL8 maintain the reference potential by the control signal DS as previously discussed in connection with FIG. **6**. The control signal BLK maintains all block selection control lines BSC1 to BSC512 to about 4.3 volts, thereby causing all word lines to be discharged to the reference potential. Upper and lower gate lines UGLi and LSGLi are also maintained at the reference potential by Xd. On the other hand, the line DCB being at "H" level causes bit lines to be discharged to the reference potential.

FIG. **17** shows a timing chart of the programming mode of the modified embodiment. Referring to FIG. **17**, the data loading operation is performed prior to time t_1. The data loading operation is performed in the same manner as that of the first embodiment as discussed in connection with FIG. **2***b*. The time period between t_1 and t_2 is for writing data into selected memory transistors. As discussed in the data loading operation of the first embodiment, bit lines corresponding to memory transistors into which logic "1" data is written are at "L" level of 0 volts while bit lines corresponding to memory transistors into which logic "0" data is written are at "H" levels of 5 volts. After the time t_1, the selected control gate line goes to the program voltage V_{pgm} of 18 volts, and unselected control gate lines go to the pass voltage V_{pas} of 10 volts as previously discussed in connection with FIG. **6**. It is now assumed that the fourth control gate line CGL4 was designated by address signals. Then, the control gate line CGL4 goes to the program voltage V_{pgm} of 18 volts and control gate lines CGL1 to CGL3 and CGL5 to CGL8 go to the pass voltage V_{pas} of 10 volts. It is also assumed that the third memory block was designated by address signal and the address signal A_{11} was "H" level. Then, the decoder **322** of FIG. **14** outputs "L" level and the block selection control line BSC3 goes to the program voltage V_{pgm} of 18 volts after the time t_1. At this time, the upper selection gate line USGL3 goes to the potential of 5 volts and the lower selection gate line LSGL3 goes to the

reference potential. Thus, the transfer transistor array 34-3 of FIG. 13*a* is turned on. On the other hand, the ground line driving circuit 320 of FIG. 15 provides the reference potential onto the lines UGSL and LGSL during the programming period. Thus, the second upper and lower selection transistors UST2 and LST2 in the upper and lower memory blocks USBK3 and LSBK3 are all nonconductive. The first lower selection line LSL1 in the lower memory block LSBK3 also goes to the reference voltage via the transfer transistor BT11, thereby causing the first lower selection transistors LST1 to be turned off. However, the first upper selection line USL1 in the upper memory block USBK3 goes to "H" level of 5 volts via the transfer transistor BT1. During the above-mentioned programming operation, the voltage relationship of significant portions may be summarized in the following TABLE 5.

TABLE 5

	Selected Memory Block	
	Selected Upper Memory Block	Unselected Lower Memory Block
Selected First Upper Selected Line USL1	5 V	—
Unselected First Lower Selected Line LSL1	—	0 V
Selected Word Line	V_{pgm} = 18 V	V_{pgm} = 18 V
Unselected Word Line	V_{pas} = 10 V	V_{pas} = 10 V
Selected Second Upper Selection Line USL2	0 V	—
Unselected Second Lower Selection Line LSL2	—	0 V
Well Electrode	0 V	0 V

Thus, during the programming operation, the high voltage applied onto word lines WL1 to WL8 causes the NAND cell charging of upper and lower memory blocks USBK3 and LSBK3. Thus, since the first upper selection line USL1 is at the potential of 5 volts, and bit lines associated with memory transistors into which logic "0" data is written are at 5 volts while bit lines associated with memory transistors into which logic "1" data is written are at the reference potential of 0 volts, first upper selection transistors in the upper memory block USBK3 which are connected with the latter memory transistors are turned on, and first upper selection transistors in the memory block USBK3 which are connected with the former memory transistors are turned off. Thus, sources, drains and channels of memory transistors in NAND cells associated with the former memory transistors go to the reference potential, and NAND cells associated with the latter memory transistors are charged to a high voltage. Consequently, during the programming period, floating gates of the former memory transistors connected with the upper word line WL4 accumulate electrons by way of the F-N tunneling, thereby changing into enhancement transistors having a threshold voltage of about 0.8 volts. That is, logic "1" data is stored. However, since channels of the latter memory transistors and junction capacitors of their sources and drains are charged with a high voltage, the programming of these memory transistors is prevented.

In the same manner, the first lower selection line LSL1 and the second lower selection line LSL2 in the unselected lower memory block LSBK3 are at the reference potential, and the first and the second lower selection transistors LST1 and LST2 which are respectively connected to the lines LSL1 and LSL2 are thereby turned off. Thus, channels of memory transistors of NAND cells in the lower memory block LSBK3 and junction capacitors of their sources and drains are charged with a high voltage so as to prevent programming.

At the time t_2, the programming operation is terminated and the clock ϕ_R stops clocking. Thus, the charge pump circuit 348 is disabled and BSC3 thereby falls to the potential of 5 volts. During the time period between t_2 and t_3, the control signal DS at "L" level causes control gate lines CGL1 to CGL8 to be grounded. Thus, word lines in the memory block SBK3 are discharged to the reference potential. During the time period between t_3 and t_4, block selection control lines BSC1 to BSC512 and upper selection gate lines USGL1 to USGL512 are discharged to the reference potential.

The programming verification operation may be performed from the time t_4 of FIG. 17. The programming verification operation is similar to that of the first embodiment. The difference as compared with the first embodiment is in that the present embodiment has the block selection control circuit for selecting one of either the upper or lower memory block in a selected memory block. If the upper memory block USBKi in a selected memory block is selected by means of the block selection control circuit of FIG. 14 in the programming verification operation, a selected block selection control line BSCi goes to the potential of about 4.3 volts, and the upper selection gate line USGLi goes to the potential of 5 volts. Then, the ground line driving circuit 320 of FIG. 15 outputs "H" level of 5 volts onto the upper selection gate line UGSL and "L" level of 0 volts onto the lower selection gate line LGSL. As discussed in connection with the first embodiment with reference to FIG. 6, in the programming verification operation, a selected control gate line is at the program verifying voltage of 0.8 volts and unselected control gate lines are at the potential of 5 volts. Thus, the line BSCi of about 4.3 volts connected to the transfer transistor array 34i of FIG. 13*a* goes to a potential of about 7 volts since the potential of 5 volts on the unselected control gate lines is transferred from drains of transfer transistors to their gates by way of capacitive coupling. This operation is also identical in a reading operation. Consequently, a selected word line in the upper memory block USBKi goes to the verifying voltage of 0.8 volts and unselected word lines go to the potential of 5 volts. The first and second upper selection lines USL1 and USL2 also go to the potential of 5 volts. Thus, second selection transistors UST2 in the block USBKi are turned on, thereby connecting NAND cells in the block USBKi to the grounded common source line CSL. However, the first and second lower selection lines LSL1 and LSL2 in the lower memory-block. LSBKi are at the reference potential and the block LSBKi are at the reference potential and the block LSBKi are at the reference potential and the block LSBKi is thereby unselected. The following programming verification and reprogramming operations are the same as operations explained in the first embodiment in connection with the timing chart during the time period between t_2 and t_4 of FIG. 12.

In the modified embodiment, programming and reprogramming techniques do not need a program inhibition voltage generator connected with the respective bit lines to inhibit programming of logic "0" programmed cells and reprogramming of successfully logic "1" programmed cells. Thus, the simplification of a peripheral circuit and the reduction of on-chip area can be accomplished. Otherwise, since the program inhibition voltage is automatically generated by the capacitive coupling technique during the programming and reprogramming operations, the programming and reprogramming operations may be executed at a

high speed. Thus, since the present embodiment employs a self-program inhibition technique, the above-mentioned advantages may be accomplished.

In the reading operation of the modified embodiment, a selected word line of 0 volts is used instead of the selected word line of 0.8 volts in the above-mentioned programming verification operation. Operation to select memory transistors in the reading operation is the same as that in the programing verification operation. Page reading, page readout sensing and the output from data output terminals are also the same as operations explained in the first embodiment in connection with FIG. 12.

Thus, EEPROMs of embodiments of the present invention as described above can be designed so as to have capabilities and reliability of improved programming, block erasing and programming verification. The peripheral circuits associated with a reading and a programming verification according to embodiments of the invention can also be used in a nonvolatile semiconductor memory with a NOR-type memory array.

What is claimed is:

1. A nonvolatile semiconductor memory comprising:

word lines formed over a surface of a semiconductor substrate;

cell units arranged on said surface to form an array, each said unit including at least one memory transistor which has source and drain regions formed in said substrate and separated by a channel region; a floating gate formed over said channel region, and a control gate formed over said floating gate and coupled to a corresponding one of said word lines, said array being divided into a plurality of memory blocks each having a plurality of cell units; and

a control circuit, responsive to an address, in a data erase mode, for applying an erase voltage to said substrate, and for floating word lines of memory blocks unselected by said address so that erasure of data in memory transistors of said unselected memory blocks is prevented by capacitive coupling of a predetermined amount of said erase voltage to said word lines of said unselected memory blocks.

2. A method for erasing data stored in a nonvolatile semiconductor memory, during a data erase mode of operation thereof, said memory comprising an array of cell units formed on a surface of a semiconductor substrate, each said cell unit including at least one memory transistor for storage of data each of said memory transistors having a floating gate and a control gate coupled to a corresponding one of a plurality of word lines, said array being divided into a plurality of memory blocks each being comprised of a plurality of cell units, said method comprising the steps of:

applying an erase voltage to said substrate;

applying a reference voltage to word lines of a selected memory block in order to erase data of memory transistors in said selected memory block; and

floating word lines of unselected memory blocks such that said data in said memory transistors of said unselected memory blocks is prevented from erasure by capacitive coupling of a predetermined amount of said erase voltage to said word lines of said unselected memory blocks.

3. A method for preventing erasure of data in memory transistors in unselected memory blocks in a nonvolatile semiconductor memory, wherein said memory comprises a multiplicity of cell units formed on a surface of a semiconductor substrate and configured in an array, each cell unit having at least one memory transistor which has a source, a drain, a floating gate, and a control gate connected to a corresponding one of a plurality of word lines, wherein said array is divided into a plurality of memory blocks each including a plurality of said cell units and word lines, said method comprising the steps of:

floating word lines of said unselected memory blocks; and

applying an erase voltage to said substrate so that data in said memory transistors of said unselected memory blocks is prevented from being erased by capacitive coupling of a predetermined quantity of said erase voltage to said word lines of said unselected memory blocks.

4. A method for preventing erasure of data in unselected cell units in a nonvolatile semiconductor memory, wherein each cell unit is formed on a surface of a semiconductor substrate and includes a plurality of memory transistors connected in series, each said memory transistor having source and drain regions formed in said substrate and separated by a channel region, a floating gate formed over said channel region to store binary data, and a control gate formed over said floating gate, respective control gates of said memory transistors of said cell unit being connected to respective ones of a plurality of word lines, said method comprising the steps of:

applying an erase voltage to said substrate; and

capacitively charging said word lines of said unselected cell units to a pretermined amount of said erase voltage.

5. An electrically erasable and programmable read-only memory comprising:

a semiconductor substrate;

an array of cell units, said cell units arranged in rows and columns on said substrate, said array being divided into a plurality of memory blocks, with each memory block being defined by at least a given one of said rows of said cell units, each of said cell units including a predetermined number of series connected memory transistors and each of said memory transistors having a floating gate and control gate;

a plurality of word lines arranged such that said control gates of memory transistors in a given row are connected to a same word line and said control gates of the memory transistors in a given column are connected to different word lines; and

a control circuit for floating word lines of unselected memory blocks and applying an erase potential to said substrate so that data in memory transistors of said unselected memory blocks is prevented from being erased by capacitive coupling of a predetermined quantity of said erase potential to said word lines of said unselected memory blocks.

6. An electrically erasable and programmable read-only memory as recited in claim 5, wherein said control circuit applies a low potential to word lines of a selected memory block thereof in order to erase data of memory transistors of said selected memory block.

7. An electrically erasable and programmable read-only memory as recited in claim 6, wherein said erase potential is a high potential and said low potential is a ground potential.

8. An electrically erasable and programmable read-only memory comprising:

a semiconductor substrate;

a multiplicity of memory transistors arranged in rows and columns, each memory transistor including a floating gate and a control gate;

a plurality of word lines each connected to said control gates of respective ones of said memory transistors in a corresponding row;

a control circuit, responsive to an address in a data erase mode, for floating word lines unselected by said address, and for applying an erase voltage to said substrate so that erasure of data in memory transistors associated with said unselected word lines is prevented by capacitive coupling of a predetermined amount of said erase voltage to said unselected word lines.

9. An electrically erasable and programmable read-only memory comprising:

a semiconductor substrate;

a multiplicity of memory transistors arranged in rows and columns on said substrate to define a plurality of cell units each of which includes a predetermined number of series-connected memory transistors, each of said memory transistors having a floating gate and a control gate;

a plurality of memory blocks being defined by respective rows of said cell units;

a plurality of word lines each connected to the control gates of the respective ones of the memory transistors in a corresponding row; and

a control circuit for floating word lines of memory blocks not required to be erased and applying an erase potential to said substrate, thereby capacitively coupling a predetermined amount of said erase potential to said floated word lines to prevent erasure of data in said memory transistors connected to said floated word lines.

* * * * *

US0056 9A

United States Patent [19]

Kim et al.

[11] Patent Number: 5,642,309

[45] Date of Patent: Jun. 24, 1997

[54] **AUTO-PROGRAM CIRCUIT IN A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE**

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[73] Assignee: **Samsung Electronics Co., Ltd.**, Suwon, Rep. of Korea

[21] Appl. No.: **526,422**

[22] Filed: **Sep. 11, 1995**

[30] **Foreign Application Priority Data**

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Jan. 24, 1995 [KR] Rep. of Korea 1144/1995

[51] **Int. Cl.**[6] **G11C 7/00**; G11C 16/04

[52] **U.S. Cl.** **365/185.22**; 365/185.2; 365/189.07; 365/189.09

[58] **Field of Search** 365/189.01, 185.01, 365/182, 218

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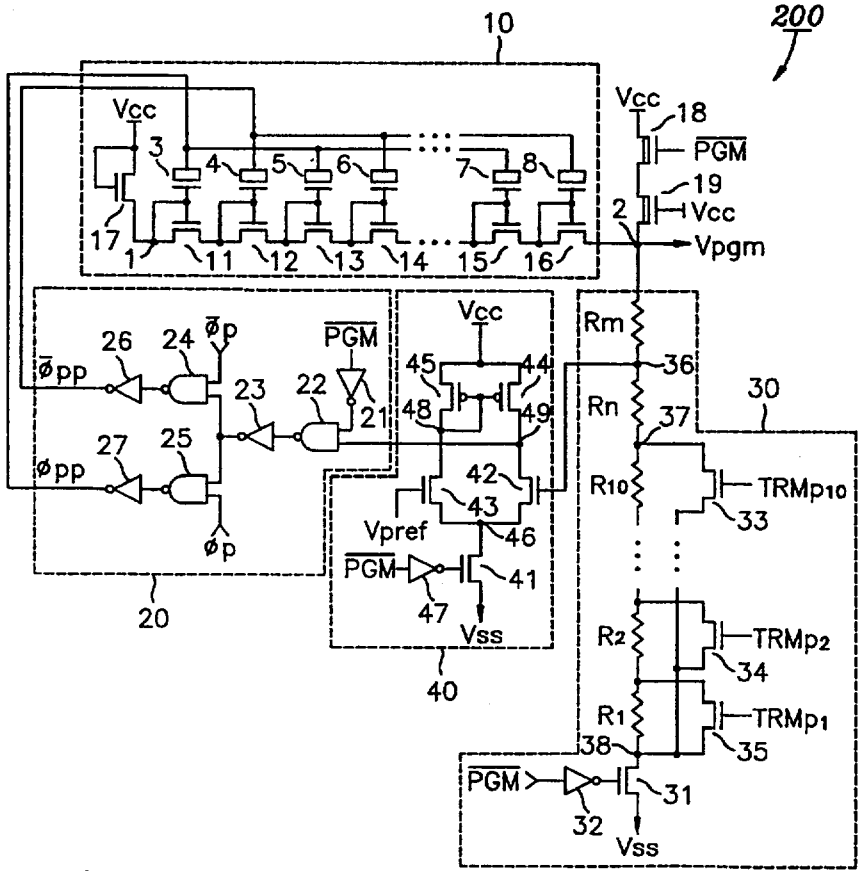
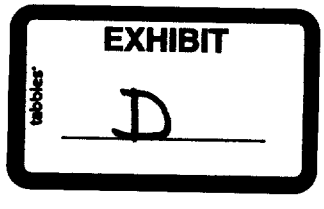
Primary Examiner—Viet Q. Nguyen
Attorney, Agent, or Firm—Cushman Darby & Cushman, IP Group of Pillsbury Madison & Sutro LLP

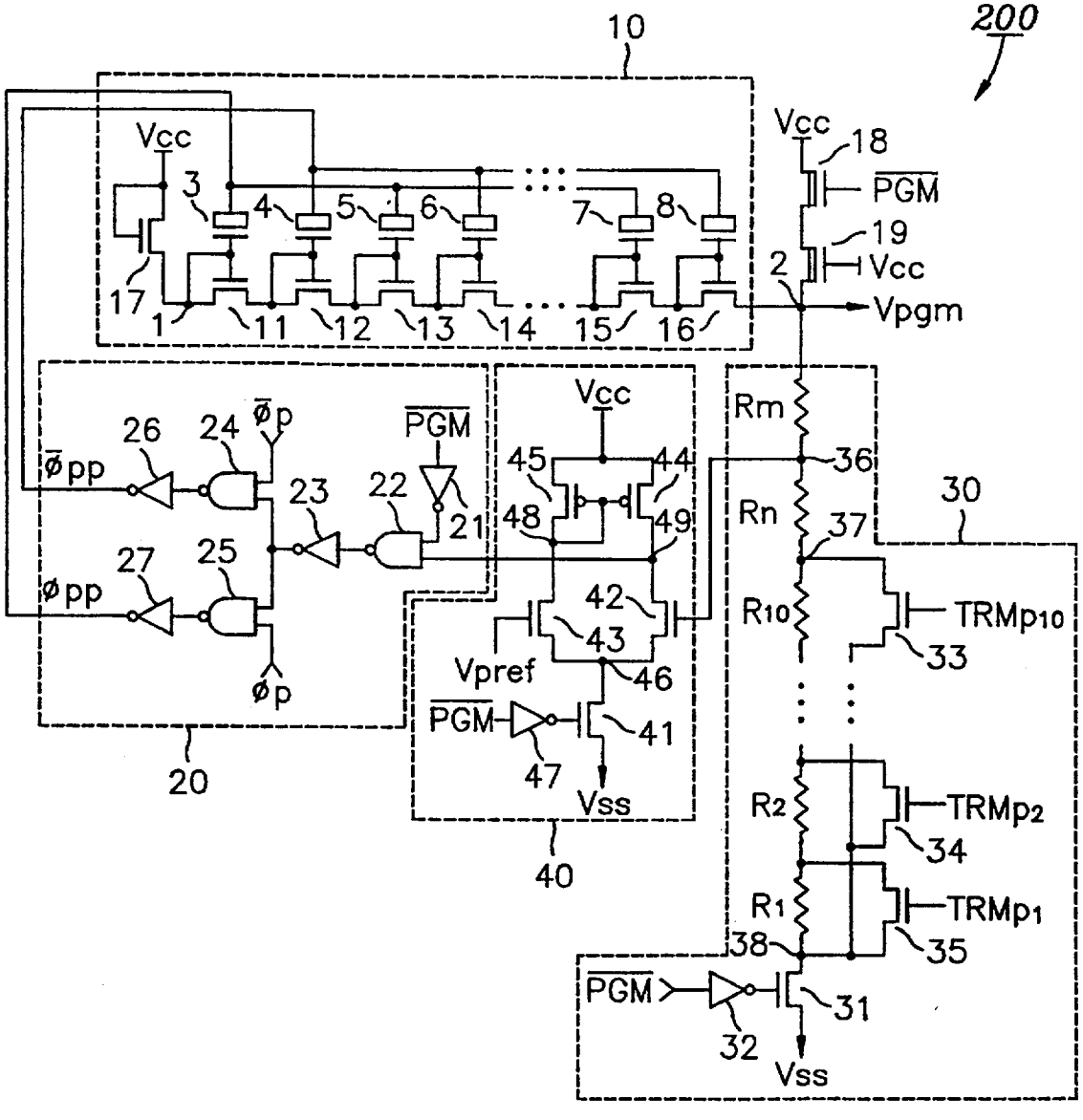
[57] **ABSTRACT**

An auto-program voltage generator in a nonvolatile semiconductor memory having a plurality of floating gate type memory cells, program circuit for programming selected memory cells, and program verification circuit for verifying whether or not the selected memory cells are successfully programmed comprises a high voltage generator for generating a program voltage, a trimming circuit for detecting the level of the program voltage to increase sequentially the program voltage within a predetermined voltage range every time the selected memory cells are not successfully programmed, a comparing circuit for comparing the detected voltage level with a reference voltage and then generating a comparing signal, and a high voltage generation control circuit for activating the high voltage generator in response to the comparing signal.

19 Claims, 10 Drawing Sheets



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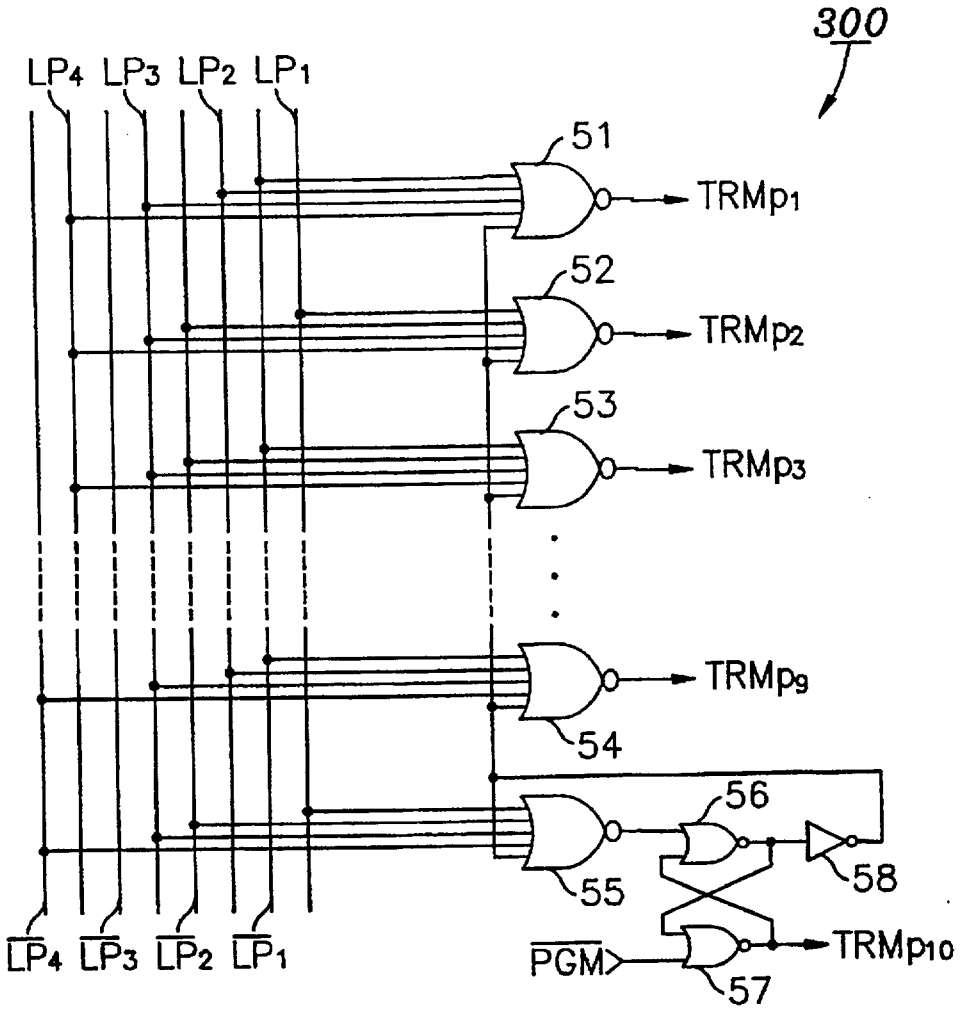
Vcc
3
4
5
6
7
8
17
1
11
12
13
14
15
16
Vcc
18
PGM
19
2
Vcc
Vpgm
Vcc
Rm
36
Rn
37
30
R10
TRMp10
33
R2
TRMp2
34
R1
TRMp1
35
38
PGM
31
32
Vss
26
24
ø̄p
ø̄pp
23
22
PGM
21
27
25
øpp
øp
20
45
44
48
49
42
43
Vpref
46
PGM
41
47
Vss
40

FIG. 1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51
TRMp1
52
TRMp2
53
TRMp3
TRMp9
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56
58
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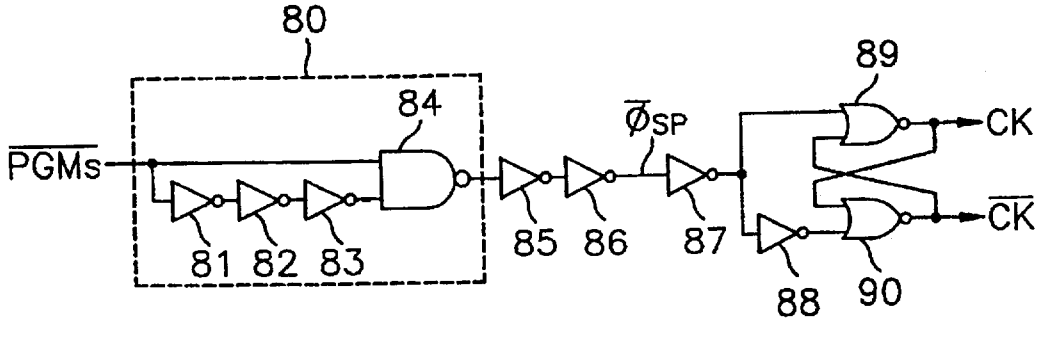
TRMp10
57
PGM
LP4 LP3 LP2 LP1

FIG. 2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PGMs
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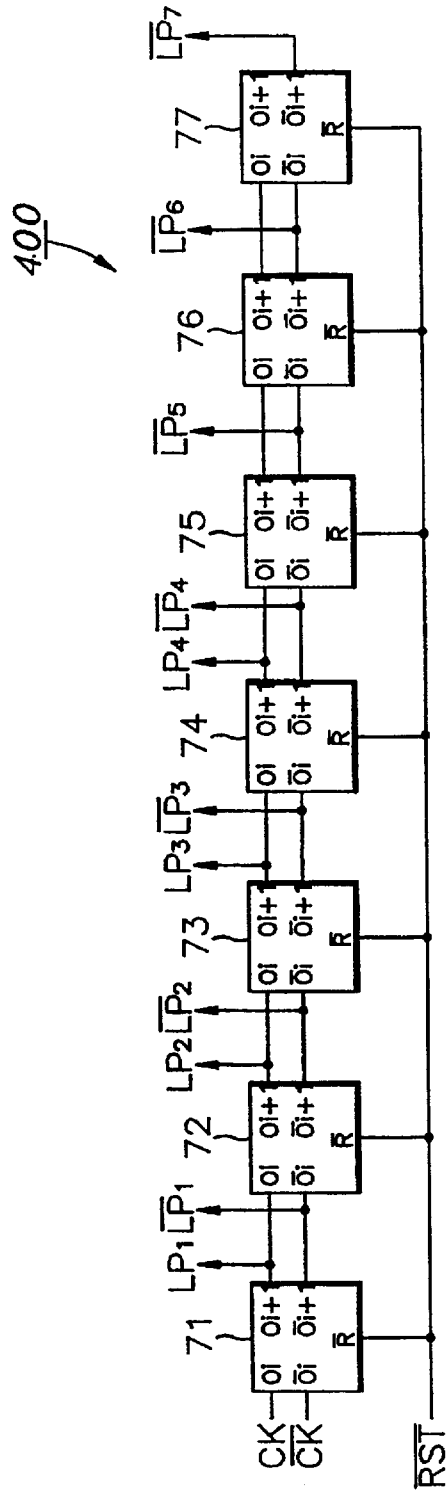
ØSP
87
89
CK
CK
88 90

FIG. 4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76
77
LP1
LP2
LP3
LP4
LP5
LP6
LP7
CK
RST

FIG. 3A

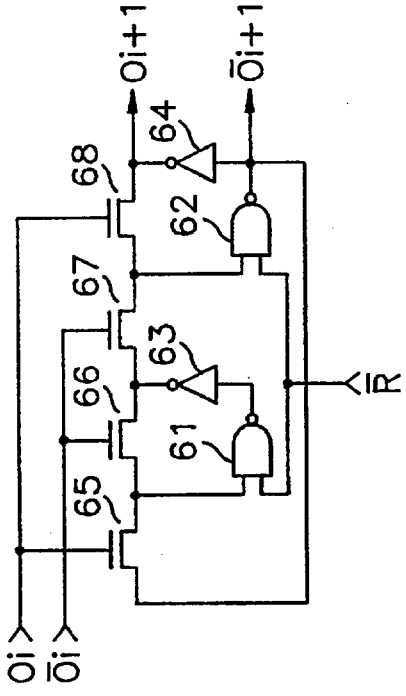

Oi+1
64
62
68
67
63
66
61
65
R
Oi

FIG. 3B

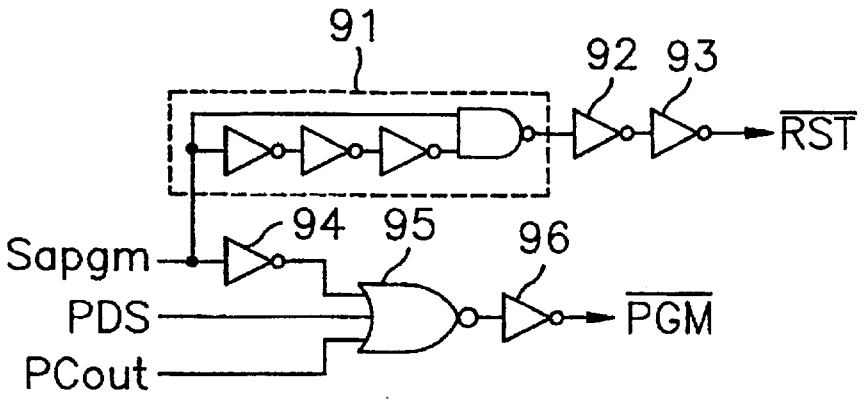
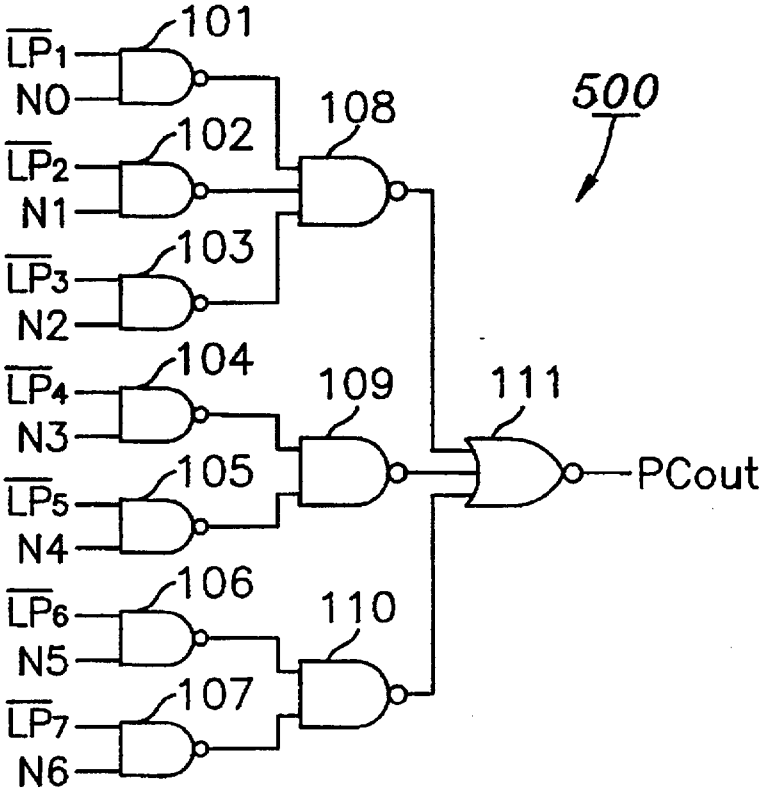

91
92
93
RST
94
95
96
Sapgm
PDS
PCout
PGM

FIG. 5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LP1
N0
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LP2
N1
103
LP3
N2
104
LP4
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LP6
N5
107
LP7
N6
108
109
110
111
500
PCout

FIG. 6

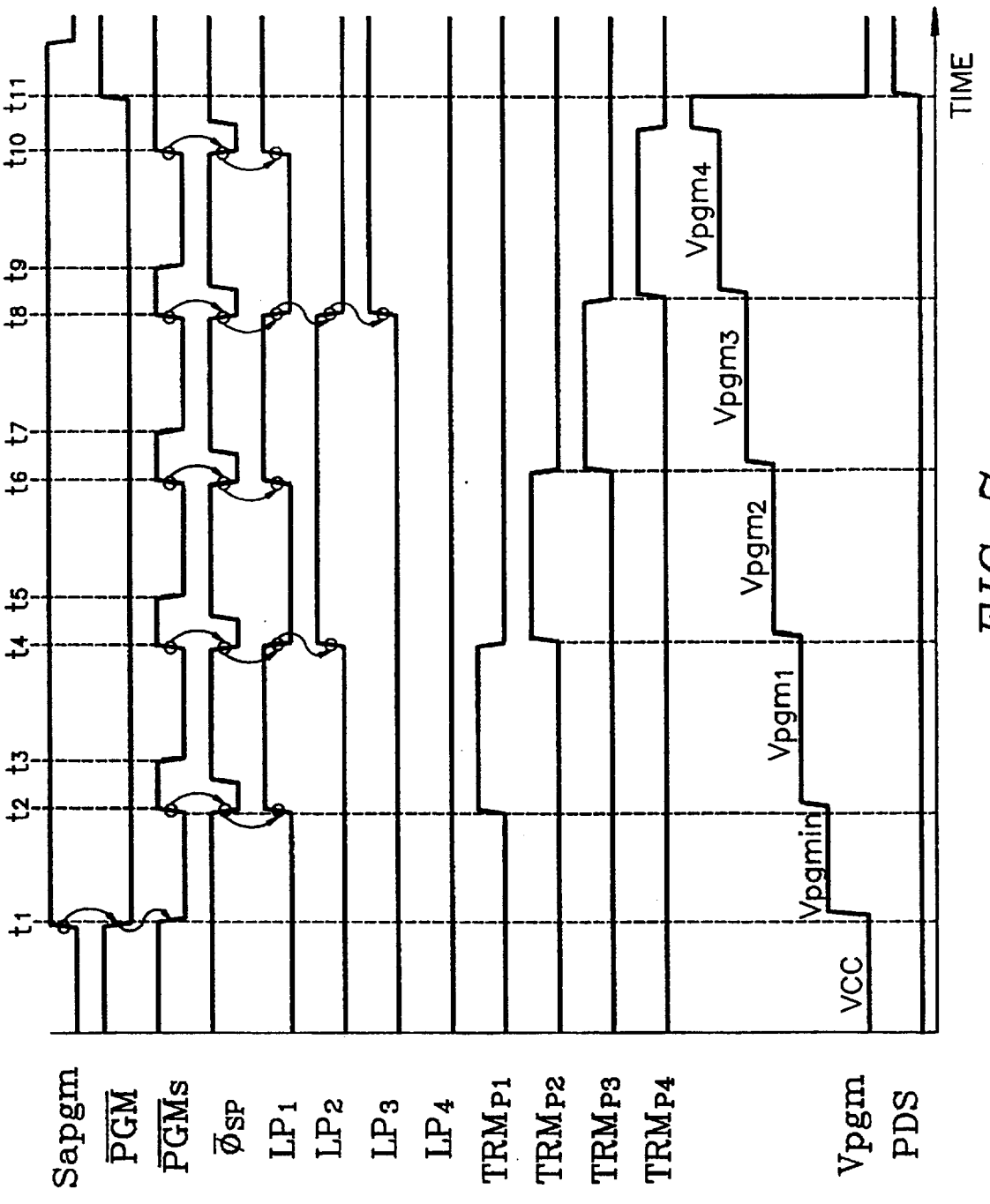

Sapgm
PGM
PGMs
ØSP
LP1
LP2
LP3
LP4
TRMP1
TRMP2
TRMP3
TRMP4
Vpgm
PDS
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
TIME
Vpgm4
Vpgm3
Vpgm2
Vpgm1
Vpgmin
VCC

FIG. 7

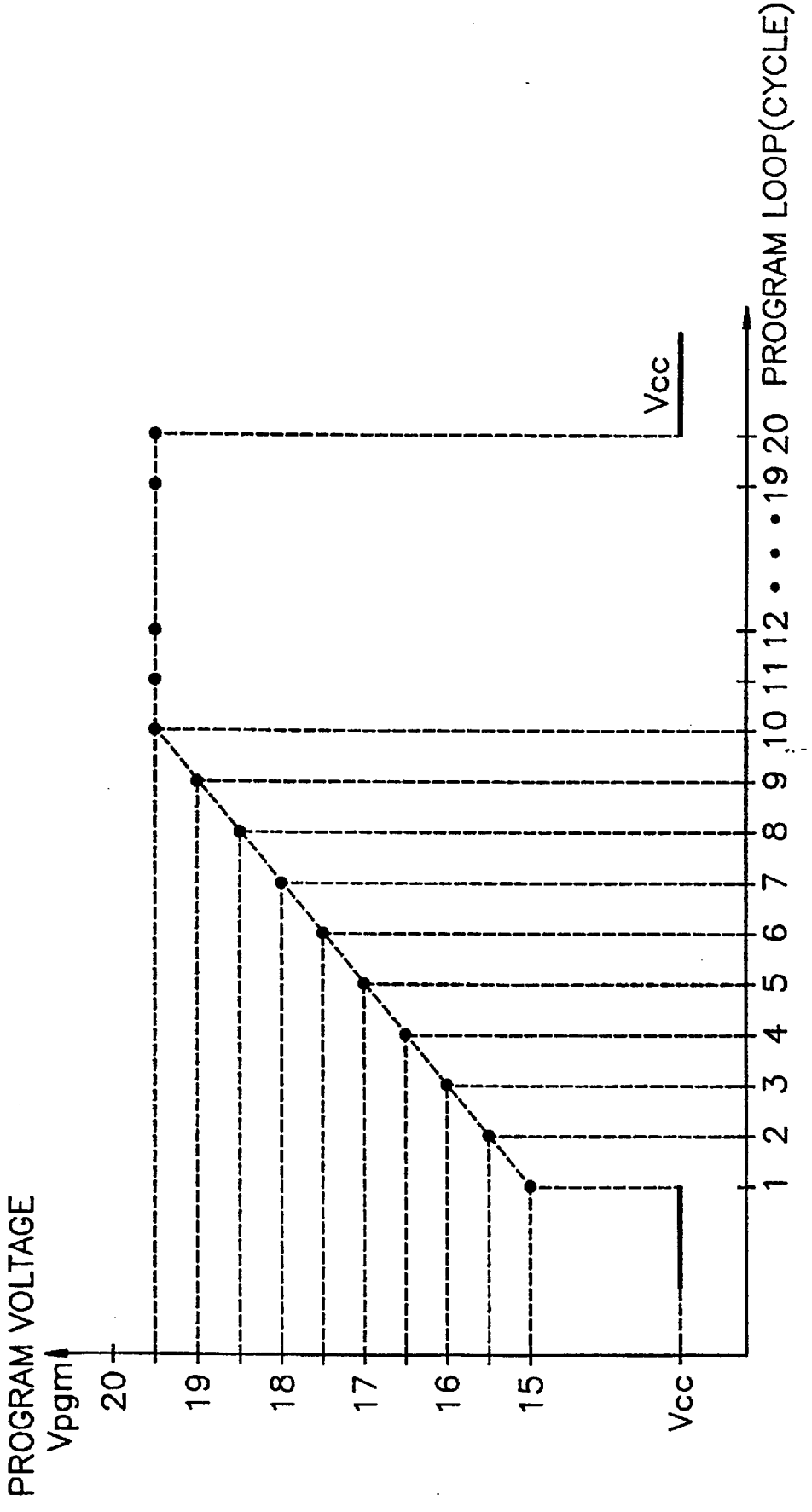
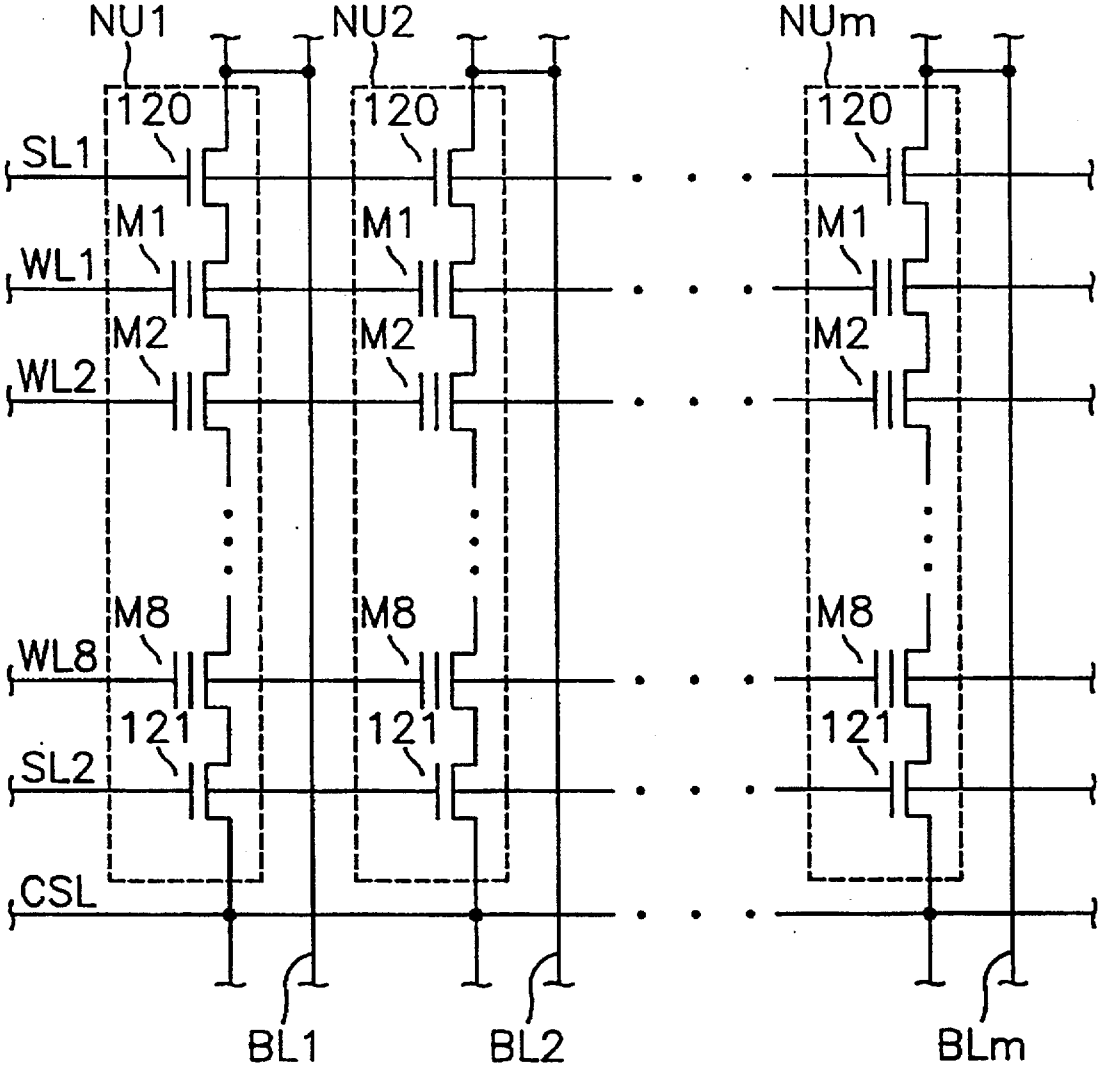

PROGRAM VOLTAGE
Vpgm
20
19
18
17
16
15
Vcc
Vcc
1 2 3 4 5 6 7 8 9 10 11 12 • • • 19 20 PROGRAM LOOP(CYCLE)

FIG. 8


NU1
NU2
NUm
120
120
120
SL1
M1
M1
M1
WL1
M2
M2
M2
WL2
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M8
M8
WL8
121
121
121
SL2
CSL
BL1
BL2
BLm

FIG. 9

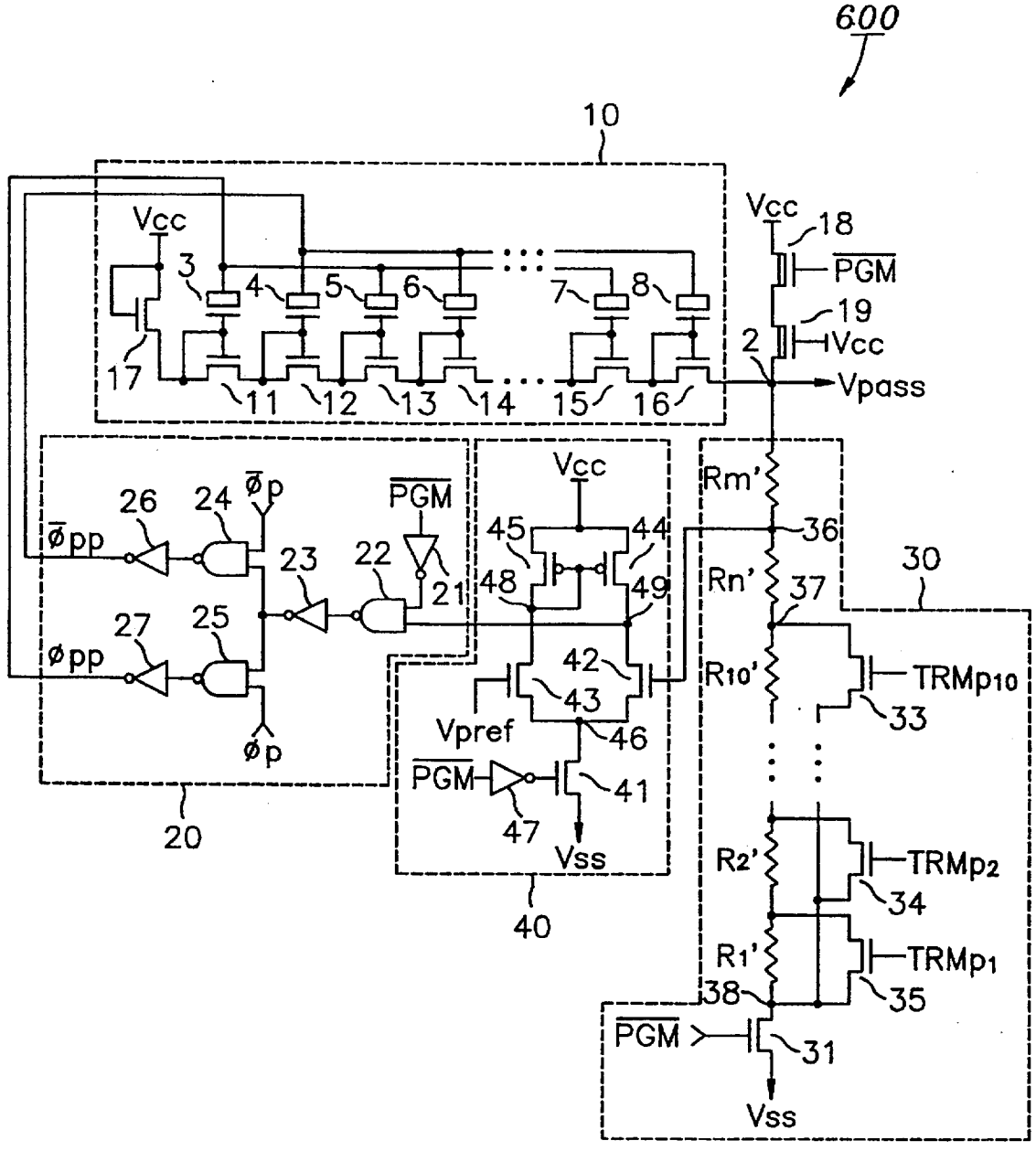
600
10
Vcc
3
4
5
6
7
8
17
11
12
13
14
15
16
Vcc
18
PGM
19
2
Vcc
Vpass
26
24
ø̄p
ø̄pp
23
22
PGM
21
27
25
øpp
øp
20
Vcc
45
44
48
49
42
43
Vpref
46
PGM
41
47
Vss
40
Rm'
36
Rn'
37
30
R10'
TRMp10
33
R2'
TRMp2
34
R1'
TRMp1
38
35
PGM
31
Vss

FIG. 10

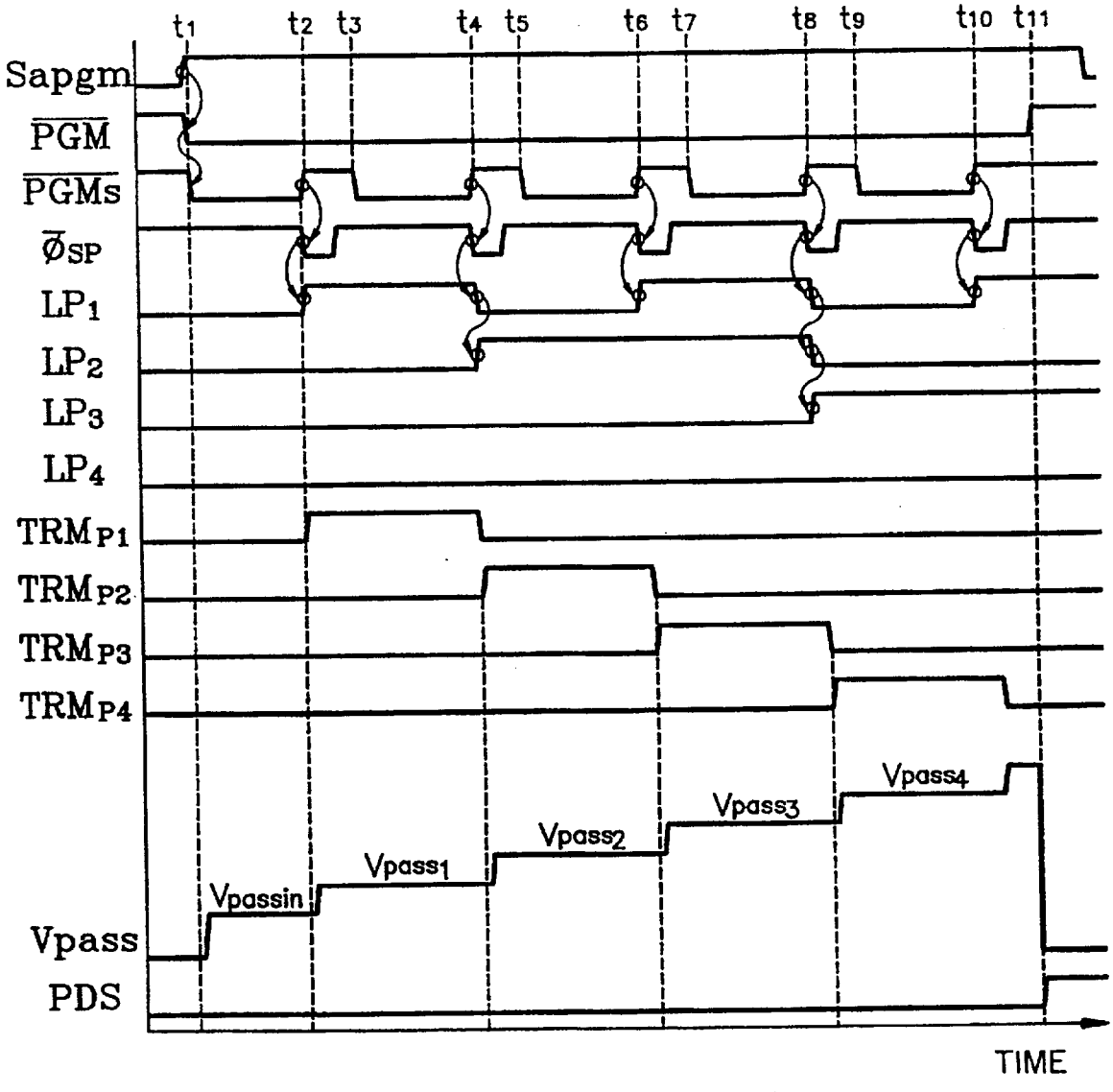
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
Sapgm
PGM
PGMs
ØSP
LP1
LP2
LP3
LP4
TRMP1
TRMP2
TRMP3
TRMP4
Vpassin
Vpass1
Vpass2
Vpass3
Vpass4
Vpass
PDS
TIME

FIG. 11

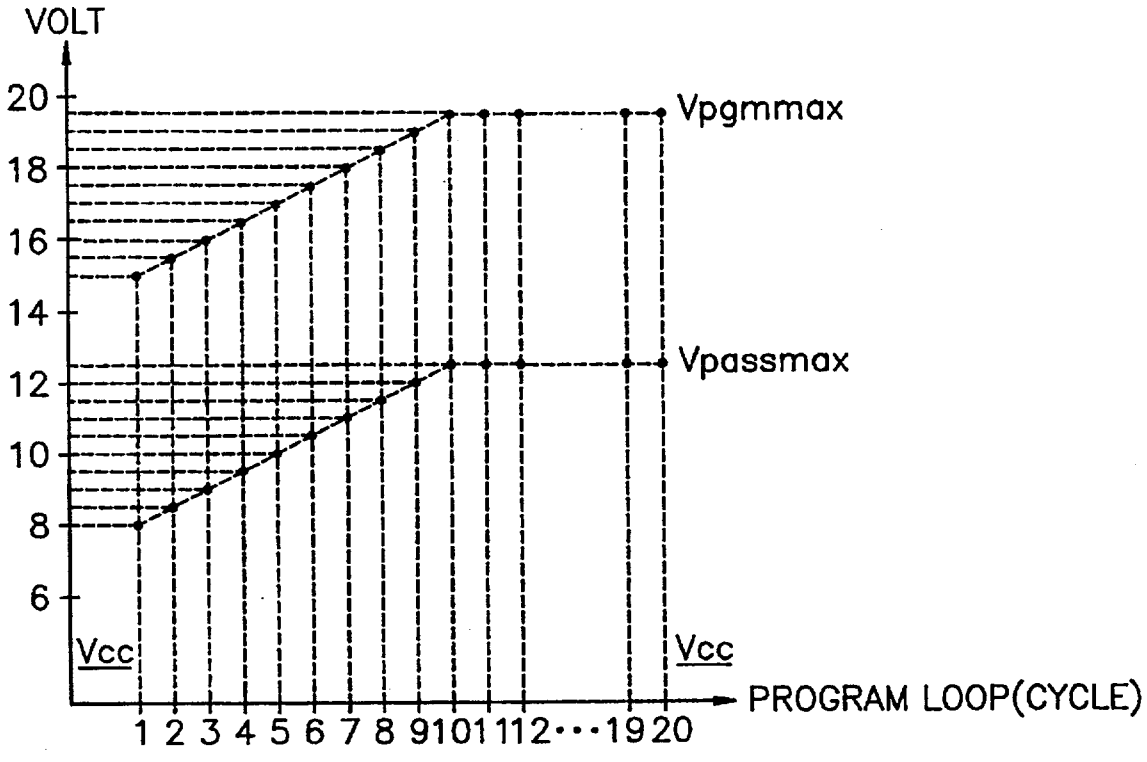
VOLT
20
18
16
14
12
10
8
6
Vpgmmax
Vpassmax
Vcc
Vcc
PROGRAM LOOP(CYCLE)
1 2 3 4 5 6 7 8 9 10 11 12 · · · 19 20

FIG. 12

AUTO-PROGRAM CIRCUIT IN A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a nonvolatile semiconductor memory device, and more particularly to an auto-program circuit in the nonvolatile semiconductor memory device.

2. Description of the Related Arts

A memory cell array with NAND structured cells has a plurality of NAND cell units arranged in a matrix with columns and rows. FIG. **9** is an equivalent circuit diagram showing a part of the memory cell array with conventional NAND structured cells. Referring to the figure, each of the NAND cell units NU1 to NUm has a first selection transistor **120** with its drain connected to the corresponding bit line and a second selection transistor **121** with its source connected to a common source line CSL. The drain-source channels of memory cell transistors M1 to M8 (hereinafter referred to as "memory cells") are serially connected between a source of the first selection transistor **120** and a drain of the second selection transistor **121**. The gates of the first selection transistors **120**, the control gates of the memory cells M1 to M8 and the gates of the second selection transistors **121** are connected to a first selection line SL1, word lines WL1 to WL8 and a second selection line SL2, respectively. The first and second selection transistors **120** and **121** and the memory cells M1 to M8 are formed in the P type well formed on the main surface of a semiconductor substrate. The source-drain common region between the source of the first selection transistor **120** and the drain of the memory cell M1, the source-drain common regions of the memory cells M1 to M8, and the drain-source common region between the drain of the second selection transistor **121** and the source of the memory cell M8 are formed in the P type well. A floating gate made of polysilicon is formed on each channel of the memory cells M1 to M8 through a tunnel oxide layer, and a floating gate made of polysilicon or of metal silicide with high melting point is formed thereon through an intermediate insulating layer. The drain regions of the first selection transistors **120** formed in the P type well are respectively connected to the corresponding bit lines made of metal silicide with high melting point or metal through openings, the source regions of the second selection transistors **121** formed in the P type well are connected to the common source line CSL made of the metal silicide with high melting point or metal. The erase operation for the memory cells is performed before programming, i.e., writing data.

The erase operation for the memory cells is performed by applying erase voltage of about 20 V to the P type well region and reference voltage, i.e., ground voltage to the word lines WL1 to WL8. With the electrons stored in the floating gates being emitted to the P type well region through the tunnel oxide layer, the memory cells are changed to enhancement mode transistors. It can be assumed that the erased memory cells store the data "1".

The programming operation for the memory cells connected to the selected word line, i.e., the writing operation of the data "0" is performed by applying program voltage of about 18 V to the selected word line and the reference voltage, i.e., the ground voltage Vss to the sources and drains of the memory cells in which the data "0" is written.

Then, the floating gates of the memory cells to be programmed accumulate the electrons thorough the tunnel oxide layers, and these memory cells are changed to the depletion mode transistors.

After programming, the program verification operation is performed to verify whether or not the selected memory cells are successfully programmed to have a predetermined constant threshold voltage value. These erase, program and program verification techniques are disclosed in the Korean Patent Publication No. 94-18870 published Aug. 19, 1994 and assigned to the present inventor.

As the capacitance of the EEPROM has become highly integrated, the size of the memory cell, such as the width and thickness of the gate oxide layer and the width and length of the channel region, has been reduced. However, variance of the manufacturing process can not secure the uniformity of the width and thickness of the gate oxide layer, intermediate insulating layer and channel region. This makes the threshold voltage values of the programmed memory cells unequal. If at least one of the programmed memory cells does not reach a desired threshold voltage, error data is read out. In order to solve such a problem, a program verification device has been proposed for verifying whether or not the selected memory cells are successfully programmed. For example, such a program verification technique is disclosed in the aforementioned Korean Patent Publication No. 94-18870. However, as the reprogram operation is performed after the program verification operation with a program voltage of constant level, the threshold voltages of the programmed memory cells are still unequal. The variance of the circumstance conditions such as a power supply voltage or an operating temperature may deteriorate the reliability of the EEPROM.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a nonvolatile semiconductor memory capable of maintaining a uniform threshold voltage of the memory cells to be programmed regardless of the variance of the operating temperature and power supply voltage.

It is another object of the present invention to provide the nonvolatile semiconductor memory capable of enhancing the reliability thereof regardless of the variance of the process.

To achieve the above objects of the present invention, an auto-program voltage generator of the nonvolatile semiconductor memory having a plurality of floating gate type memory cells, a program circuit for programming the selected memory cells, and a program verification circuit for verifying whether or not the selected memory cells are successfully programmed, comprises a high voltage generator for generating a program voltage, a trimming circuit for detecting the level of the program voltage so as to sequentially increase the program voltage within a predetermined voltage range every time the selected memory cells are not successfully programmed, a comparing circuit for comparing the detected voltage level with a reference voltage and then generating a comparing signal, and a high voltage generation control circuit for activating the high voltage generator in response to the comparing signal.

BRIEF DESCRIPTION OF THE DRAWINGS

In the detailed description of the preferred embodiment of the present invention presented below, reference is made to the accompanying drawings, in which:

FIG. 1 is a diagram illustrating a program voltage generator according to a preferred embodiment of the present invention;

FIG. 2 is a diagram illustrating a trimming signal generator according to the preferred embodiment of the present invention;

FIG. 3A is a diagram illustrating a binary counter according to the preferred embodiment of the present invention;

FIG. 3B is a diagram illustrating each stage in the binary counter of FIG. 3A;

FIG. 4 is illustrates a clock signal generator for generating a clock signal for driving the binary counter of FIG. 3A;

FIG. 5 is a diagram illustrating a control signal generator according to the preferred embodiment of the present invention;

FIG. 6 is a diagram illustrating a loop counter according to the preferred embodiment of the present invention;

FIG. 7 is a timing diagram showing the operations of each part of the circuits related to the program voltage generator according to the preferred embodiment of the present invention;

FIG. 8 is a diagram showing the relation between the program loop and the program voltage according to the preferred embodiment of the present invention;

FIG. 9 is an equivalent circuit diagram showing a part of the memory cell array with conventional NAND structured memory cells;

FIG. 10 is a schematic circuit diagram showing a pass voltage generator according to the preferred embodiment of the present invention;

FIG. 11 is a timing diagram showing the operation of each part of the circuits related to the pass voltage generator according to the preferred embodiment of the present invention; and

FIG. 12 is a diagram showing the relation between the program loop and the program voltage and pass voltage according to the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

N-channel transistors of depletion mode (hereinafter referred to as "D type transistors") having a threshold voltage of −1.8 V, N-channel MOS transistors of enhancement mode (hereinafter referred to as "N type transistors") having the threshold voltage of 0.7 V, and P-channel MOS transistors (hereinafter referred to as "P type transistors") having the threshold voltage of −0.9 V are employed in the present invention.

FIG. 1 illustrates a program voltage generator **200**. In the figure, a high voltage generator **10** functions to generate a program voltage Vpgm in response to a charge pumping signal ϕpp and its complementary signal $\overline{\phi}pp$ outputted from a high voltage generation control circuit **20**. The high voltage generator **10** is a well-known circuit for generating the program voltage Vpgm higher than the power supply voltage Vcc by utilizing a charge pumping method. The high voltage generator **10** comprises an N type transistor **17** for providing an initial voltage Vcc-Vth to a node **1**, N type transistors **11** to **16** having their own channels serially connected between the node **1** and an output node **2**, and MOS capacitors **3** to **8** respectively connected to the gates of the N type transistors **11** to **16**. The gates of the N type transistors **11** to **16** are respectively connected to their drains, and the drain-source common nodes of odd MOS capacitors **3**, **5**, and **7** and the drain-source common nodes of even MOS capacitors **4**, **6**, and **8** are connected to the charge pumping signal ϕpp and its complementary signal $\overline{\phi}pp$, respectively.

The channels of the D type transistors **18** and **19** are serially connected between the output node **2** of the high voltage generator **10** and the power supply voltage Vcc, and the gates thereof are respectively connected to a program control signal $\overline{PGM}$ and the power supply voltage Vcc. At the completion of the program operation, the D type transistors **18** and **19** function to discharge the program voltage Vpgm to the power supply voltage Vcc.

A trimming circuit **30** for sequentially increasing the program voltage Vpgm during the program operation is connected to the output node **2**. Between the ground voltage Vss and the output node **2** is connected the trimming circuit **30** in which the channel of an N type transistor **31** and the resistors R_1 to R_{10}, R_n and R_m are serially connected one another and the gate of the N type transistor **31** is connected to the program control signal $\overline{PGM}$ through an inverter **32**. A connection node **37** between the resistors R_n and R_{10} is connected to a connection node **38** between the resistor R_1 and the drain of the N type transistor **31** through the channel of an N type transistor **33**. The connection nodes between the resistors R_{10} to R_1 are respectively connected to the connection node **38** through the channels of the transistors **34** and **35**. The gates of the transistors **33** to **35** are respectively connected to the trimming signals TRM_{P1} to TRM_{P10}. The transistors **33** to **35** are bypass means for bypassing the resistors R_1 to R_{10}, sequentially.

A comparing circuit **40** functions to compare the reference voltage Vpref with the voltage V_{36} of the connection node **36** between the resistors R_m and R_n. In the comparing circuit **40**, the channel of a transistor **41** is connected between the ground voltage Vss and a common node **46**, and the gate thereof is connected to the program control signal $\overline{PGM}$ through an inverter **47**. A first branch in which the channels of the P type transistor **44** and N type transistor **42** are serially connected and a second branch in which the channels of the P type transistor **45** and N type transistor **43** are serially connected are connected in parallel between the power supply voltage Vcc and the common node **46**. The gates of the P type transistors **44** and **45** are commonly connected each other and are also connected to a connection node **48** between the P type transistor **45** and the N type transistor **43**. The reference voltage Vpref, i.e., about 1.67 V is applied to the gate of the N type transistor **43**. The gate of the N type transistor **42** is connected to the common node **36**. The connection node **49** between the P type transistor **44** and the N type transistor **42** serves as an output terminal of the comparing circuit **40**. The comparing circuit **40** outputs the logic "low" state if the voltage V_{36}>the reference voltage Vpref, and outputs the logic "high" state if V_{36}<Vpref.

The high voltage generation control circuit **20** is connected between the comparing circuit **40** and the high voltage generator **10** and functions to control the program voltage Vpgm to maintain a predetermined constant voltage level. The high voltage generation control circuit **20** comprises a NAND gate **22** having one input connected to the connection node **49** and the other connected to the program control signal $\overline{PGM}$ through an inverter **21**. The first inputs of the NAND gates **24** and **25** receive the output of the NAND gate **22** through an inverter **23**, and the second inputs thereof respectively receive the clock pulses $\overline{\phi}p$ and $\overline{\phi}p$ from a ring oscillator (not shown). At this time, the clock pulses $\overline{\phi}p$ and $\overline{\phi}p$ have the frequency of about 8 MHz. The NAND gates **24** and **25** output the charge pumping signals $\overline{\phi}pp$ and $\overline{\phi}pp$ through inverters **26** and **27**.

If V_{36}>Vpref, the high voltage generation control circuit **20** is inactivated, and if V_{36}<Vpref, it becomes activated. Thus, if the program voltage Vpgm increases, the voltage

V_{36} also increases. Therefore, the high voltage generation control circuit **20** is inactivated and thus the high voltage generator **10** reduces the program voltage Vpgm. On the other hand, if the program voltage Vpgm is too low, the high voltage generator **10** increases the program voltage Vpgm. Hence, the program voltage Vpgm maintains a constant voltage level by the control of the high voltage generation control circuit **20**.

At the turn off state of the transistors **33** to **35**, the initial program voltage Vpgmin on the output node **2** can be represented as follows:

$$Vpgmin = Vpref\left(1+\frac{R_m}{R_1+R_2+\ldots+R_{10}+R_n+R_m}\right). \quad (1)$$

At the turn on state of the transistor **35**, the program voltage V_{pgm1} on the output node **2** can be represented as follows:

$$V_{pgm1} = Vpref\left(1+\frac{Rm}{R_2+\ldots+R_{10}+R_n+R_m}\right). \quad (2)$$

At the turn on state of the transistor **34**, the program voltage V_{pgm2} on the output node **2** can be represented as follows:

$$V_{pgm2} = Vpref\left(1+\frac{R_m}{R_3+\ldots+R_{10}+R_n+R_m}\right). \quad (3)$$

As can be seen from the above equations, when the transistors **35** to **33** are sequentially turned on, the program voltage on the output node **2** are sequentially increased. Accordingly, by sequentially performing the program and program verification operations with increasing the program voltage sequentially within a predetermined voltage range, i.e., from 15 V to 19.5 V, the memory cells having constant threshold voltages regardless of various changes such as the change of the process and the change of the circumstance conditions can be implemented.

FIG. **2** is a trimming signal generator **300** for generating trimming signals which sequentially increase the program voltage Vpgm with sequentially turning on the transistors **35** to **33** in FIG. **1**. The trimming signal generator **300** has a plurality of NOR gates **51** to **55** which receive the combinations of the output signals LP_1 to LP_4 of a binary counter and their complementary signals $\overline{LP_1}$ to $\overline{LP_4}$. The output of the NOR gate **55** is coupled to one input of a NOR gate **56** in a flip-flop. The output of the NOR gate **56** is applied to the NOR gates **51** to **55** through an inverter **58**, and also to one input of a NOR gate **57**. The other input of the NOR gate **57** in the flip-flop is coupled to the program control signal $\overline{PGM}$, and the output thereof is connected to the trimming signal TRM_{P10} and also to the other input of the NOR gate **56**. During the program operation, the flip-flop composed of the NOR gates **56** and **57** latches the trimming signal TRM_{P10} to the logic "high" state if the NOR gate **55** is selected, i.e., the NOR gate **55** outputs the logic "high" state. The inverter **58** provides the output of the NOR gate **56** as a feedback signal. Thus, the NOR gates **56** and **57** and the inverter **58** are latch means for latching the trimming signals TRM_{P1} to TRM_{P10} to the logic "low" state. Therefore, if the selected memory cell is not successfully programmed even after the completion of the tenth program verification operation, the program operations thereafter maintain the increased maximum program voltage Vpgmmax level, i.e., 19.5 V according to the preferred embodiment of the present invention. As the maximum program voltage Vpgmmax is selected as the value capable of preventing the junction break down and the break down of the gate oxide layer of the memory cell, it should be noted that the present invention is not limited to the maximum program voltage level of 19.5 V. In addition, the present invention employs 10 trimming signals, however, it is not limited thereto, either. However, it is desired that the program voltage Δv to be increased every program operation should be below 1 V, preferably below 0.5 V.

FIG. **3A** shows the binary counter and FIG. **3B** a schematic circuit diagram of each stage in the binary counter of FIG. **3A**.

Referring to FIG. **3B**, the channels of N type transistors **65** to **68** are serially connected between an output terminal oi+1 and its complementary output terminal $\overline{oi}$+1, the gates of the transistors **66** and **67** are commonly connected to a complementary clock input terminal $\overline{oi}$, and the gates of the transistors **65** and **68** to the clock input terminal oi. An inverter **64** is connected between the output terminal oi+1 and its complementary output terminal $\overline{oi}$+1, a second input of a NAND gate **61** is coupled to a connection node between the transistors **65** and **66**, and the output thereof to a connection node between the transistors **66** and **67** through an inverter **63**. A second input of the NAND gate **62** is coupled to a connection node between the transistors **67** and **68**, and the output thereof to the complementary output terminal $\overline{oi}$+1. Thus, if the reset signal of logic "low" state is applied to a reset terminal $\overline{R}$, the output terminal oi+3 becomes the logic "low" state and its complementary output terminal $\overline{oi}$+1 becomes the logic "high" state. In addition, every time the input of the input terminal oi goes from the logic "high" state to the logic "low" state, the output state of the output terminal oi+1 is changed.

The binary counter **400** of FIG. **3A** is composed of 7 stages serially connected one another. The reset terminal $\overline{R}$ is coupled to the reset signal $\overline{RST}$, and the clock input terminal oi and its complementary clock input terminal $\overline{oi}$ at the first stage are respectively connected to the clock signal CK and its complementary clock signal $\overline{CK}$. The 7 stages **71** to **77** output complementary counting signals $\overline{LP_1}$ to $\overline{LP_7}$, and the 4 stages **71** to **74** output the counting signals LP_1 to LP_4. Every time the clock signal CK goes to the logic "low" state, the counting signals LP_1 to LP_4 are counted up and the complementary counting signals $\overline{LP_1}$ to $\overline{LP_7}$ are counted down.

FIG. **4** is a circuit diagram showing a clock signal generator for generating the clock signal to be provided to the binary counter **400** of FIG. **3A**. In the figure, a program and verification signal $\overline{PGMs}$ is generated from a timer (not shown) in response to the program control signal $\overline{PGM}$. The clock signal generator comprises a short pulse generator **80** composed of inverters **81** to **83** and a NAND gate **84**, inverters **85** to **88**, and NOR gates **89** and **90**. The NOR gates **89** and **90** are comprised in a flip-flop. The short pulse generator **80** generates the short pulse of logic "low" state when the program and verification signal $\overline{PGMs}$ goes to the logic "high" state.

FIG. **5** is a schematic circuit diagram of a control signal generator for generating the reset signal $\overline{RST}$ and the program control signal $\overline{PGM}$. The control signal generator of FIG. **5** generates the reset signal $\overline{RST}$ through a short pulse generator **91** and inverters **92** and **93** in response to an auto-program flag signal Sapgm outputted from a command register (not shown). The auto-program flag signal Sapgm is applied to a first input of a NOR gate **95** through an inverter **94**, a program detection signal PDS to a second input thereof and a loop counting signal PCout to a third input thereof. The NOR gate **95** outputs the program control signal $\overline{PGM}$

through an inverter **96**. The program detection signal PDS is generated according to the program verification operation. If all the selected memory cells have been successfully programmed, the program detection signal PDS becomes the logic "high" state. On the contrary, if at least one of the selected memory cells has not been successfully programmed, the program detection signal PDS becomes the logic "low" state. Such a program verification technique is disclosed in the aforementioned Korean Patent Publication No. 94-18870.

FIG. **6** shows a loop counting circuit **500** for generating the loop counting signal PCout. The loop counting circuit **500** is a logic circuit composed of NAND gates **101** to **110** and a NOR gate **111**. The complementary counting signals $\overline{LP_1}$ to $\overline{LP_7}$ are applied from the binary counter **400** to the NAND gates **101** to **107**, respectively. The terminals **N0** to N6 are connected to the ground voltage Vss or to the power supply voltage Vcc according to the loop counting frequency. As the loop counting frequency is set to 20 according to the preferred embodiment of the present invention, the terminals N2 and N5 are connected to the power supply voltage Vcc, and the remaining terminals **N0**, **N1**, N3, N4, and N6 are connected to the ground voltage Vss.

The auto-program circuit according to the preferred embodiment will be described with reference to the timing diagram of FIG. **7**.

As shown in FIG. **7**, the auto-program operation starts in response to the transition of the auto-program flag signal Sapgm from the logic "low" state to the logic "high" state. As the program detection signal PDS and the loop counting signal PCout are in the logic "low" state at the beginning of the auto-program operation, the control signal generator generates the program control signal $\overline{PGM}$ of logic "low" state in response to the transition of the auto-program flag signal Sapgm from the logic "low" state In the logic "high" state. In addition, in response to the auto-program flag signal Sapgm which goes to the logic "high" state, the short pulse generator **91** generates the short pulse of logic "low" state and thereby the binary counter **400** of FIG. 3A is reset. As shown in FIG. **7**, the timer (not shown) generates the program and verification signal $\overline{PGMs}$ in response to the transition of the program control signal from the logic "high" state to the logic "low" state. The program and verification signal $\overline{PGMs}$ is the clock pulse which has the logic "low" state of 30 μsec and the logic "high" state of 10 μsec when the program control signal $\overline{PGM}$ is in the logic "low". The duration when the program control signal remains the logic "low" state is for the program operation, and the duration when the program control signal remains the logic "high" state is for the program verification operation.

At time t_1 of FIG. **7**, in response to the transition of the program control signal $\overline{PGM}$ from the logic "high" state to the logic "low" state, the program voltage generator **200** of FIG. **1** is enabled. That is, the transistor **41** is turned on, thus activating the comparing circuit **40**, and the transistor **31** is turned on, thus activating the trimming circuit **30**. At the beginning of the operation, as $Vpref > V_{36}$, the comparing circuit **40** outputs the logic "high" state. Hence, the inverter **23** outputs the logic "high" state and thereby the high voltage generation control circuit **20** generates the charge pumping signal ϕpp and its complementary signal $\overline{\phi pp}$. Thus, the high voltage generator **10** generates the gradually increasing high voltage by the signals ϕpp and $\overline{\phi pp}$. The program voltage Vpgm increases until the voltage V_{36} at the connection node **36** reaches the reference voltage Vpref. Consequentially, the program voltage Vpgm maintains the initial program voltage Vpgmin shown in the above-described equation (1). The technique for programming the selected memory cells with the program voltage Vpgm is disclosed in the Korean Patent Publication No. 94-18870.

At time t_2, the program and verification signal $\overline{PGMs}$ goes to the logic "high" state, and the program verification operation for the programmed memory cells is performed during the time between t_1 and t_2. In response to the program and verification signal $\overline{PGMs}$ which goes to the logic "high" state at time t_2, the short pulse generator **80** of FIG. **4** generates the short pulse and the inverter **86** generates the short pulse signal $\overline{\phi sp}$ of logic "low" state. The clock signal CK is generated as a similar signal to the short pulse signal $\overline{\phi sp}$. Then, the binary counter **400** of FIG. 3A makes the counting signal LP_1 the logic "high" state as shown in FIG. **7**. Thereby, the NOR gate **51** of FIG. **2** generates the trimming signal TRM_{P1} of logic "high" state. Thus, with the turn on state of the transistor **35** of FIG. **1**, the resistor R_1 is bypassed, and the voltage V_{36} at the connection node **36** becomes smaller than the reference voltage Vpref. As a result, the high voltage generation control circuit **20** is activated and the high voltage generator **10** generates the increased program voltage V_{pgm1} as shown in the above equation (2).

If the selected memory cells are not successfully programmed during the program verification operation between the time t_2 and t_3, i.e., the duration of 10 μsec, reprogram operation is automatically performed with the increased program voltage V_{pgm1} during the time between t_3 and t_4.

At time t_4, if the program and verification signal $\overline{PGMs}$ goes to the logic "high" state, the short pulse generator **80** of FIG. **4** generates the short pulse of logic "low" state, and the inverter **86** outputs the short pulse $\overline{\phi sp}$ of logic "low" state as shown in FIG. **7**. The clock signal CK becomes the short pulse of logic "low" state, and the counting signals LP_1 and LP_2 of the binary counter **400** become the logic "low" and logic "high" states, respectively. Thus, the NOR gate **52** of FIG. **2** generates the trimming signal TRM_{P2} which goes to the logic "high" state. In response to the trimming signal TRM_{P2} of logic "high" state, the resistors R_1 and R_2 of FIG. **1** are bypassed, and the voltage V_{36} at the connection node **36** becomes smaller than the reference voltage Vpref. Hence, the high voltage generation control circuit **20** is activated, and thereby the high voltage generator **10** generates the program voltage V_{pgm2} as shown in the above equation (3).

If the selected memory cells are not successfully programmed regardless of the reprogram operation, the program operation is performed again during the time between t_5 and t_6. In the same way, with the sequential increase of the program voltage, the program and program verification operations are automatically performed until all the selected memory cells are successfully programmed.

The timing diagram of FIG. **7** shows the case that the selected memory cells are successfully programmed at the fifth program operation. After the completion of the fifth program operation, the program detection signal PDS indicating that the selected memory cells have been successfully programmed goes to the logic "high" state at the program verification operation between the time t_{10} and t_{11}. Thereby, the control signal generator of FIG. **5** makes the program control signal $\overline{PGM}$ logic "high" state, and the circuits related to the program like a ring counter (not shown) are inactivated. After about 2.5 μsec after the program control signal $\overline{PGM}$ goes to the logic "high" state, the auto-program flag signal Sapgm becomes the logic "low" state. It is possible to

detect how many program loops are occurred during the 2.5 μsec with the complementary counting signals $\overline{LP_1}$ to $\overline{LP_7}$ outputted from the binary counter **400**.

FIG. **8** is a diagram showing the relation between the program loop and the program voltage according to the preferred embodiment of the present invention. Referring to FIG. **8**, the program operations for the selected memory cells can be performed as much as 20 times. The program voltage Vpgm sequentially increases from 15 V to 19.5 V by 0.5 V until the tenth program operation. During the eleventh to twentieth program operations, the program voltage Vpgm maintains the maximum constant voltage level Vpgmmax of 19.5 V by the latch operation of the flip-flop composed of the NOR gates **56** and **57**. If the selected memory cells are not successfully programmed after the twentieth program operation, the loop counting circuit **500** of FIG. **6** generates the loop counting signal PCout which goes to the logic "high" state, and thereby the control signal generator of FIG. **5** generates the program control signal $\overline{PGM}$ which goes to the logic "high" state, thus stopping the generation of the program voltage Vpgm.

As described above, the auto-program voltage generator generates the program voltage which increases sequentially within a predetermined voltage range depending on the program loop according to the present invention. The program voltage is supplied to the selected word line. However, the variance of the threshold voltage and the stress of the memory cells which should not be programmed among the memory cells connected to the selected word line should be prevented.

In the program operation of the conventional technique, the pass voltage Vpass, i.e., a constant voltage of 10 V is applied to the unselected word lines. For example, assuming that the word line WL2 is selected, the maximum program voltage Vpgmmax increased according to the program loop, i.e., 19.5 V is applied to the selected word line WL2, the memory cell M2 within the NAND cell unit NU2 should be programmed as data "0", and the memory cell M2 within the NAND cell unit NU1 should be kept as the erase state, i.e., data "1", the power supply voltage Vcc of 5 V is applied to the first selection line SL1, the constant pass voltage Vpass of 10 V to the unselected word lines WL1 and WL3 to WL8, and the ground voltage Vss to the second selection line SL2 during the program operation. At the same time, the ground voltage Vss is applied to the bit line BL2 related to the memory cell M2 which is to be programmed as the data "0" within the NAND cell unit NU2, and the power supply voltage Vcc of 5 V is applied to the bit line BL1 related to the memory cell M2 which should be in the erase state, i.e., the data "1" within the NAND cell unit NU1. Then, the first selection transistor **120** within the NAND cell unit NU2 is turned on and thereby the memory cell M2 within the NAND cell unit NU2 is programmed as the data "0". However, as the power supply voltage Vcc of 5 V is applied to the bit line BL1 connected to the NAND cell unit NU1 and to the gate of the first selection transistor **120** within the NAND cell unit NU1 and the pass voltage Vpass of 10 V is applied to the control gate of the memory cell M1 within the NAND cell unit NU1, the source of the first selection transistor **120** is charged with the pass voltage Vpass, and thereby the first selection transistor **120** is turned off. Thus, the source and drain of the memory cell M2 within the NAND cell unit NU1 are charged with the pass voltage Vpass (=10 V), and the increased program voltage of 19.5 V is abruptly applied to the control gate of the memory cell M2. Therefore, the memory cell M2 within the NAND cell unit NU1 receives the voltage stress of 9.5 V and thereby the thin tunnel oxide layer due to the variance of the manufacturing process or the intermediate insulating layer is broken down. Meanwhile, the threshold voltage of the memory cell M2 within the NAND cell unit NU2 is varied. Therefore, the application of the constant pass voltage Vpass to the unselected word lines deteriorates the reliability of the EEPROM. To solve such a problem, the preferred embodiment of the present invention will be described with reference to FIGS. **10** to **12**.

FIG. **10** shows a pass voltage generator for generating the pass voltage to be applied to the unselected word lines. Referring to the figure, the pass voltage generator **600** has the same structure as the program voltage generator **200** of FIG. **1** except that the values of the resistors R_1' to R_{10}', R_n' and R_m' in the pass voltage generator **600** are different from those of the resistors R_1 to R_{10}, R_n and R_m in the program voltage generator **200**, and that the pass voltage Vpass instead of the program voltage Vpgm is outputted from the output node **2**. The control signal generators shown in FIGS. **2** to **6** are also employed to control the pass voltage generator **600**. The pass voltage generator **600** generates the pass voltage Vpass which increases sequentially from the initial pass voltage Vpassin of 8 V to the maximum pass voltage Vpassmax of 12.5 V according to the program loop. The generation of the increasing pass voltage Vpass can be implemented by using the proper values of the resistors R_1' to R_{10}', R_n' and R_m'. The operations of the pass voltage generator **600** are identical to those of the program voltage generator **200** except the value of the pass voltage Vpass, and such will not be described. The control signal generators shown in FIGS. **2** to **6** are employed in the pass voltage generator **600** of FIG. **10**, and such will not be described, either.

FIG. **11** is a timing diagram for describing the operations of the pass voltage generator of FIG. **10**. FIG. **11** is identical to FIG. **7** except that the pass voltage Vpass is generated instead of the program voltage Vpgm.

FIG. **12** is a diagram showing the relation between the program voltage Vpgm and the pass voltage Vpass according to the program loop. As can be seen in the figure, the voltage difference between the program voltage Vpgm and the pass voltage Vpass maintains 5 V until the tenth program operation. Such a voltage difference can be set properly according to the structure or properties of the memory cells to prevent the insulation break down or the variance of the threshold voltage of the memory cells which should not be programmed.

As described above, since the auto-program voltage generator and the pass voltage generator according to the present invention generate the program voltage and pass voltage which increase sequentially within a predetermined voltage range, the reliability of the chip can be enhanced without the break down of the insulating layer or the variance of the threshold voltage of the memory cells which should not be programmed. In addition, it is possible to achieve a uniform threshold voltages, and to enhance the performance of the chip regardless of the change in process and the circumstance condition.

What is claimed is:

1. An auto-program voltage generator in a nonvolatile semiconductor memory having a plurality of floating gate type memory cells, program means for programming selected memory cells, and program verification means for verifying whether or not said selected memory cells are successfully programmed, said auto-program voltage generator comprising:

a high voltage generator for generating a program voltage;

a trimming circuit for causing said program voltage to increase sequentially within a predetermined voltage range every time one of said selected memory cells is not successfully programmed, said trimming circuit sequentially outputting a detected voltage level signal corresponding to said sequentially increasing program voltage;

a comparing circuit for comparing said detected voltage level signal with a reference voltage and then generating a comparing signal when said detected voltage level signal is less than said reference voltage; and

a high voltage generation control circuit for activating said high voltage generator in response to said comparing signal.

2. The auto-program voltage generator according to claim 1, wherein said trimming circuit comprises a plurality of resistors serially connected between a program voltage generation terminal of said high voltage generator and a second reference voltage, and a plurality of transistors for respectively bypassing each of said plurality of resistors in order to increase sequentially said program voltage.

3. The auto-program voltage generator according to claim 1, wherein said trimming circuit comprises a plurality of bypass means to increase sequentially said program voltage.

4. The auto-program voltage generator according to claim 3, further comprising a trimming signal generator connected to said plurality of bypass means, for generating trimming signals that are respectively supplied to each of said bypass means and allow for increasing sequentially said program voltage.

5. The auto-program voltage generator according to claim 4, wherein said trimming signal generator comprises latch means for generating a constant voltage for each of said trimming signals after said program voltage has been sequentially increased.

6. The auto-program voltage generator according to claim 4, further comprising a binary counter connected to said trimming signal generator, for sequentially activating said plurality of bypass means.

7. The auto-program voltage generator according to claim 5, further comprising a binary counter connected to said trimming signal generator, for sequentially activating said plurality of bypass means.

8. The auto-program voltage generator according to claim 7, further comprising a loop counting circuit for stopping the generation of said program voltage in response to counting signals outputted from said binary counter.

9. An auto-program voltage generating method of a non-volatile semiconductor memory which performs sequentially program and program verification operations, said sequential program using a program voltage that is sequentially increased within a predetermined voltage range and then maintained at a constant voltage level when programming a selected memory cell that is not successfully programmed.

10. The method according to claim 9, wherein said constant voltage level is set to prevent junction break down and break down of a gate oxide layer of memory cells.

11. The method according to claim 9, wherein said predetermined voltage range is from about 15 V to 19.5 V.

12. The auto-program voltage generator according to claim 1, where said sequentially increasing program voltage increases in increments that are each less than 1 volt.

13. The auto-program voltage generator according to claim 1, wherein said sequentially increasing program voltage increases in increments that are each less than 0.5 volts.

14. The method according to claim 9, where said sequentially increasing program voltage increases in increments that are each less than 1 volt.

15. The method according to claim 9, wherein said sequentially increasing program voltage increases in increments that are each less than 0.5 volts.

16. The method according to claim 11, where said sequentially increasing program voltage increases in increments that are each less than 1 volt.

17. The method according to claim 11, wherein said sequentially increasing program voltage increases in increments that are each less than 0.5 volts.

18. The auto-program voltage generator according to claim 1, wherein said memory cells are programmed in one of two states and said sequentially increasing program voltage is used to change each selected memory cell from one of said states to another of said states.

19. The method according to claim 9, wherein said memory cells are programmed in one of two states and said sequentially increasing program voltage is used to change each selected memory cell from one of said states to another of said states.

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